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April 1988

**Development of
Heterojunction Power
MISFETs**

Texas Instruments, Inc.

Sponsored by
Defense Advanced Research
Projects Agency
ARPA Order No. 4766



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15 September 1986 - 15 September 1987

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1 December 1987

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SECTION I
INTRODUCTION

The objective of this program is to develop the material, device designs, and circuit technologies for heterojunction power MISFETs capable of high-efficiency power operation at 60 GHz and 94 GHz. The use of a wide bandgap, undoped AlGaAs layer as the gate insulator is expected to provide higher gate-drain breakdown voltage and higher output power than are possible with conventional MISFETs. The charge transport layer is an undoped layer that has good transport properties. Device performance is further improved by the charge accumulation at the quantum well. The developed devices should be suitable for monolithic integration into fully dense phased arrays. The first year of this program has been dedicated to optimizing the MISFET device structure. In the remaining years of the contract the monolithic amplifier will be designed and fabricated based on the MISFETs. The performance goals of the transistor amplifier are listed in Table. 1.

Table 1
Transistor Performance Goals

Parameter	Intermediate Goals		Final Goals		
Frequency (GHz)	60	94	60	94	94
Output Power (mW)	100	30	200	30	100
Power-Added Efficiency (%)	20	15	20	30	20
Associated Gain (dB)	6	6	5	6	5

SECTION II

NUMERICAL EVALUATION OF MATERIAL STRUCTURES

Various layer structures of the quantum well MISFETs have been evaluated using the one-dimensional numerical model, which can predict the potential and charge distributions in the composite layers. The model is based on the Fermi screening approximation. The Fermi-Dirac charge distribution has been approximated using the Joyce-Dixon equation. Figure 1 shows calculated results for a normal structure quantum well MISFET. Figure 1(a) shows the material structure, which consists of five epilayers: undoped AlGaAs (insulation layer), undoped InGaAs (quantum well channel), GaAs (spacer layer), n⁺ GaAs layer (charge-providing layer), and GaAs buffer. Figure 1(b) shows the potential distribution in the structure when the gate is forward-biased to 0.95 V (Schottky barrier high is 1 V), and Figure 1(c) shows the electron distribution. It is seen that all the electrons are confined in the quantum well, which is undoped InGaAs. Therefore, the charge transport properties are comparable to the 2-D gas of the pseudomorphic HEMT layer. Because the square well confines charges at both edges, the sheet carrier density is about two times higher than the single well (HEMT layer). The structure has a doped sheet carrier density of $1.5 \times 10^{12}/\text{cm}^2$, and 37% of the charge is accumulated from the MISFET structure at the bias point. The sheet carrier density can be increased further by using a more highly doped n-GaAs layer.

Figures 2 through 4 show the other variations. The structure in Figure 2 has n-AlGaAs bottom layers. Because of the large bandgap discontinuity, the charge accumulation is large, about 72%. However, this structure is harder to grow, since the material structure is inverted (AlGaAs bottom layer). Figure 3 shows the GaAs/AlGaAs system. This structure is lattice-matched at the expense of smaller conduction band discontinuity. Figure 4 shows a structure with doped layers in both sides of the well. This structure has 32% more charge in the well than the structure with one doped layer (Figure 1). These quantum well layers should be suitable charge transport layers for millimeter-wave FETs.

(a) Material Structure

Thickness	Composition	Doping	Electron Density
20 nm	$\text{Al}_{0.40}\text{Ga}_{0.60}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$3.11 \times 10^4 \text{ cm}^{-2}$
15 nm	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$2.18 \times 10^{12} \text{ cm}^{-2}$
2 nm	GaAs	$1.0 \times 10^{10} \text{ cm}^{-3}$	$2.05 \times 10^{10} \text{ cm}^{-2}$
5 nm	GaAs	$3.0 \times 10^{18} \text{ cm}^{-3}$	$1.53 \times 10^{11} \text{ cm}^{-2}$
100 nm	GaAs	$1.0 \times 10^{13} \text{ cm}^{-3}$	$3.31 \times 10^{11} \text{ cm}^{-2}$

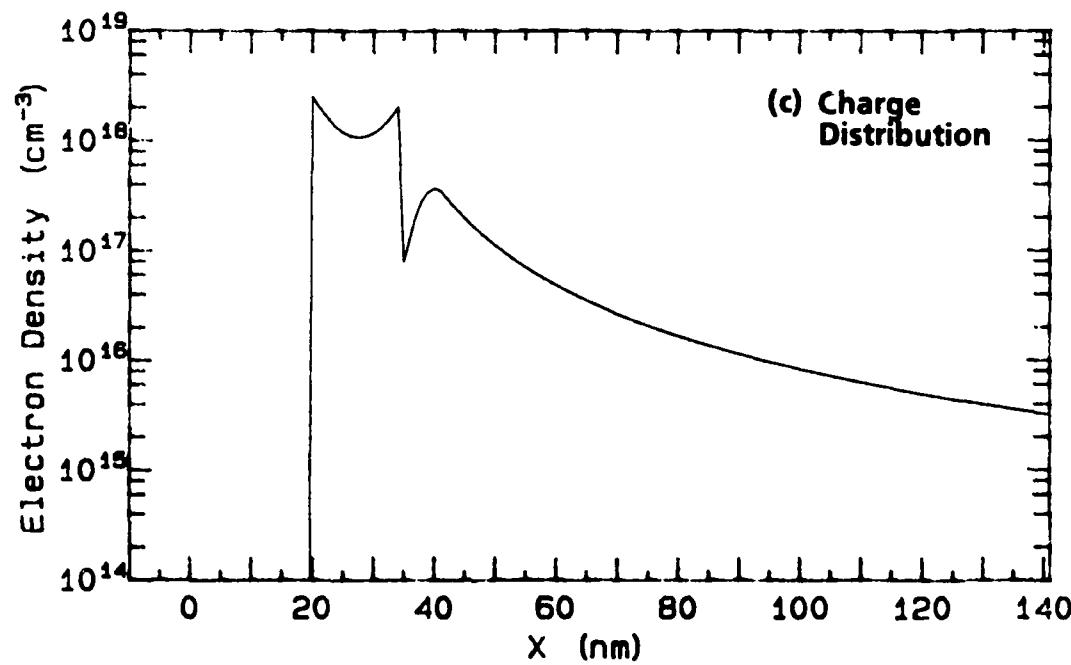
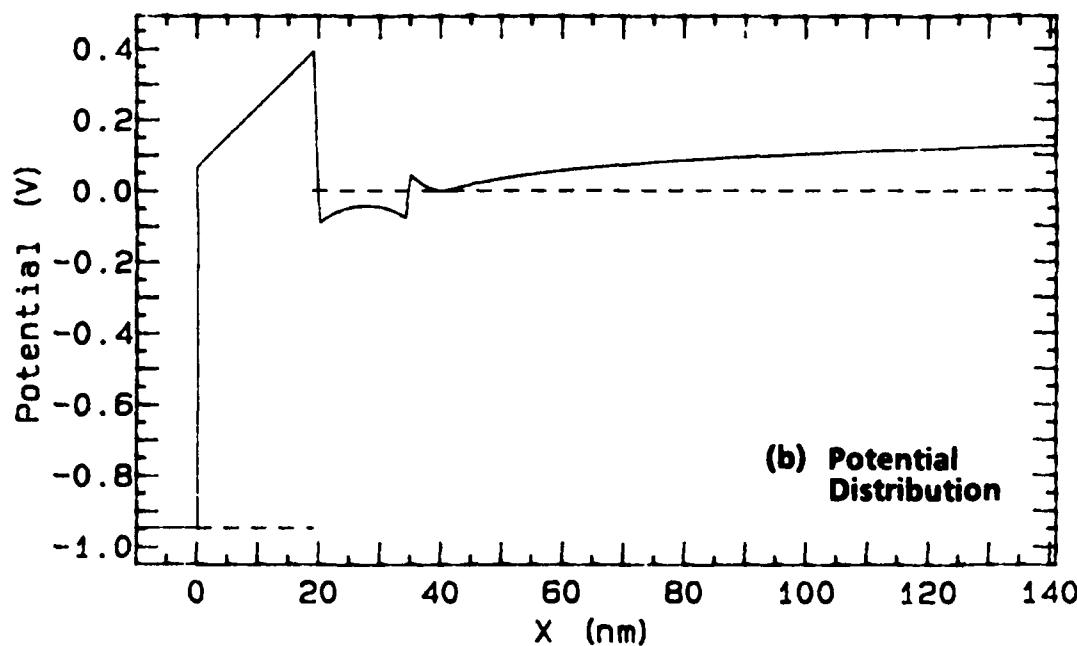


Figure 1. Quantum well MISFET with normal structure. (a) Material structure; (b) potential distribution; (c) charge distribution.

(a) Material Structure

Thickness	Composition	Doping	Electron Density
20 nm	$\text{Al}_{0.40}\text{Ga}_{0.60}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$3.14 \times 10^4 \text{ cm}^{-2}$
15 nm	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$2.58 \times 10^{12} \text{ cm}^{-2}$
2 nm	$\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$4.06 \times 10^8 \text{ cm}^{-2}$
5 nm	$\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$	$3.0 \times 10^{18} \text{ cm}^{-3}$	$7.28 \times 10^9 \text{ cm}^{-2}$
100 nm	$\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{13} \text{ cm}^{-3}$	$3.55 \times 10^{10} \text{ cm}^{-2}$

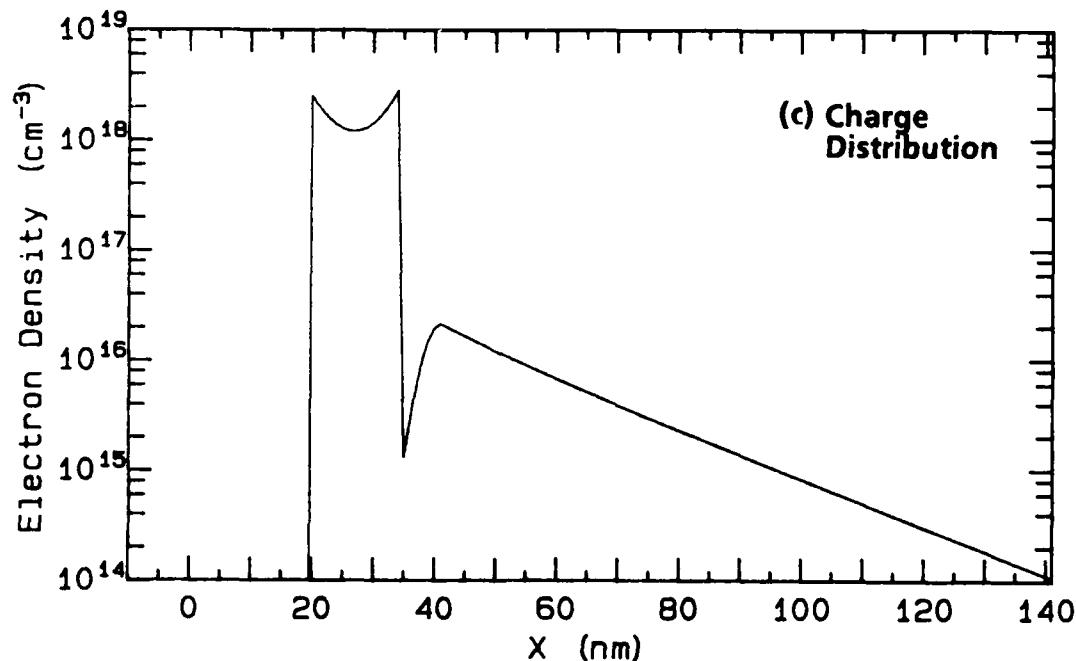
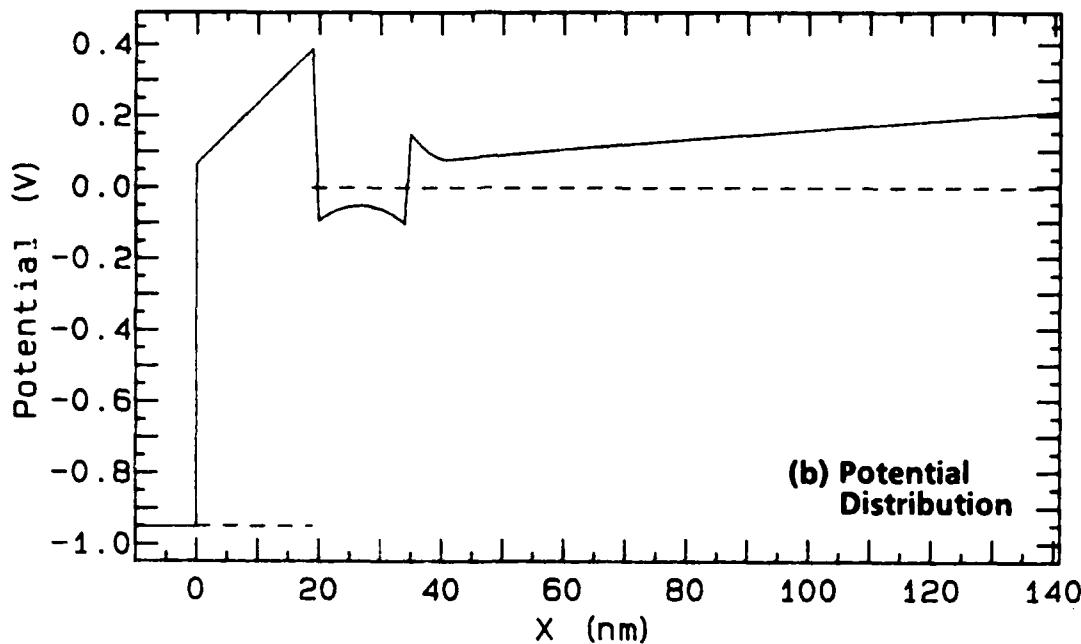


Figure 2. Quantum well MISFET with inverted structure (AlGaAs bottom layer). (a) Material structure; (b) potential distribution; (c) charge distribution.

(a) Material Structure

Thickness	Composition	Doping	Electron Density
20 nm	$\text{Al}_{0.40}\text{Ga}_{0.60}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$5.03 \times 10^4 \text{ cm}^{-2}$
15 nm	GaAs	$1.0 \times 10^{10} \text{ cm}^{-3}$	$1.83 \times 10^{12} \text{ cm}^{-2}$
2 nm	$\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$1.76 \times 10^{10} \text{ cm}^{-2}$
5 nm	$\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$	$3.0 \times 10^{18} \text{ cm}^{-3}$	$1.35 \times 10^{11} \text{ cm}^{-2}$
100 nm	$\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{13} \text{ cm}^{-3}$	$2.49 \times 10^{11} \text{ cm}^{-2}$

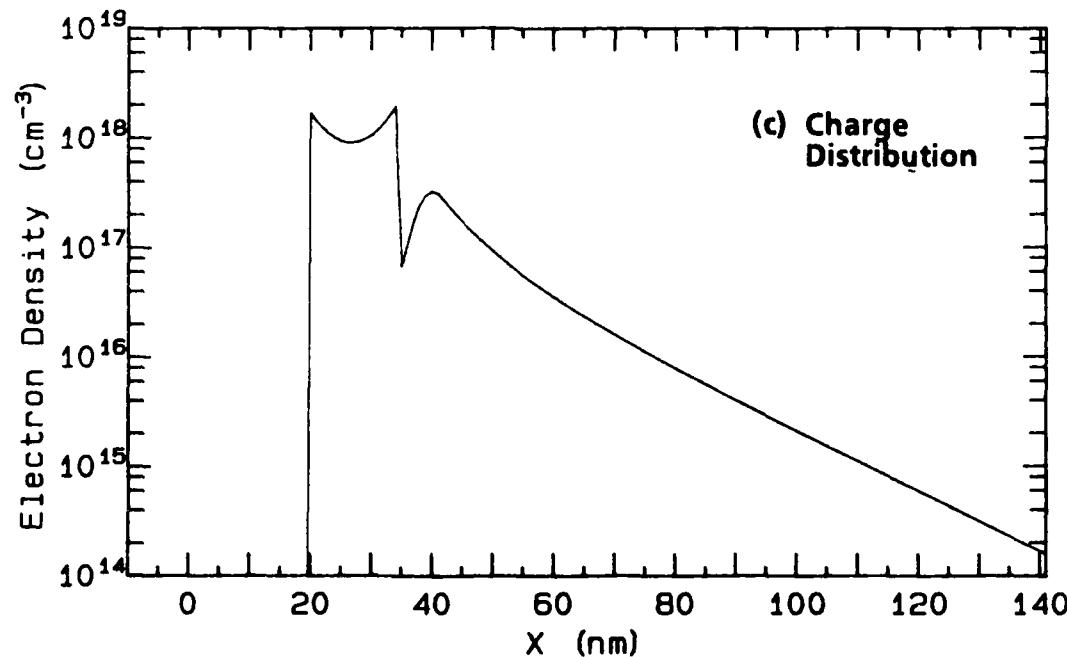
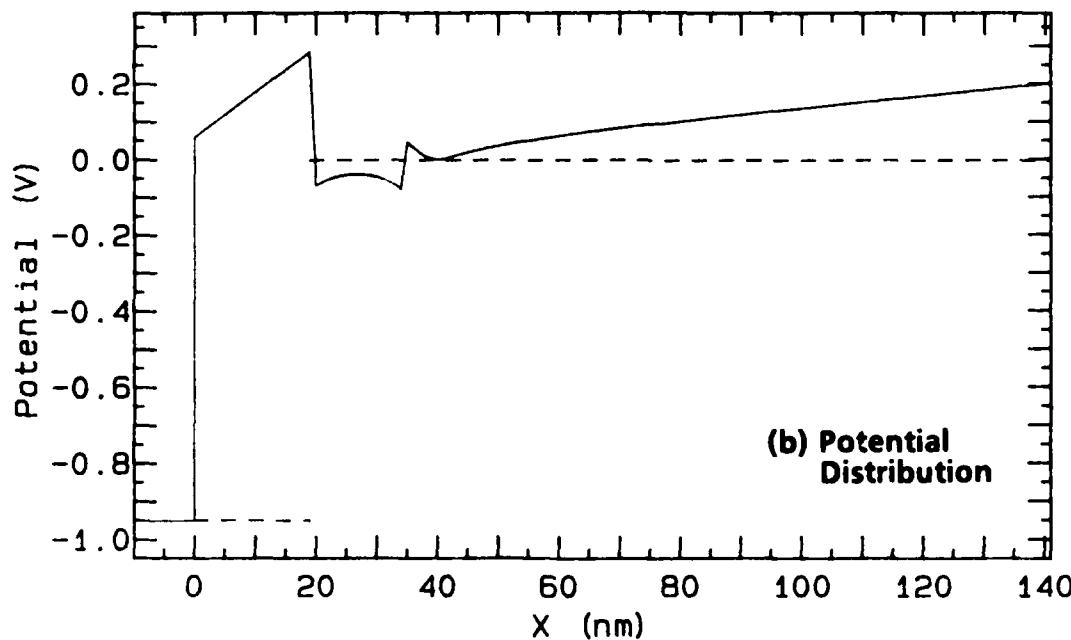


Figure 3. Quantum well MISFET with GaAs channel. (a) Material structure; (b) potential distribution; (c) charge distribution.

(a) Material Structure

Thickness	Composition	Doping	Electron Density
20 nm	$\text{Al}_{0.40}\text{Ga}_{0.60}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$8.11 \times 10^4 \text{ cm}^{-2}$
5 nm	$\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$	$3.0 \times 10^{18} \text{ cm}^{-3}$	$1.21 \times 10^{11} \text{ cm}^{-2}$
2 nm	$\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$2.31 \times 10^9 \text{ cm}^{-2}$
15 nm	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$2.88 \times 10^{12} \text{ cm}^{-2}$
2 nm	GaAs	$1.0 \times 10^{10} \text{ cm}^{-3}$	$2.28 \times 10^{10} \text{ cm}^{-2}$
5 nm	GaAs	$3.0 \times 10^{18} \text{ cm}^{-3}$	$1.56 \times 10^{11} \text{ cm}^{-2}$
100 nm	GaAs	$1.0 \times 10^{13} \text{ cm}^{-3}$	$3.41 \times 10^{11} \text{ cm}^{-2}$

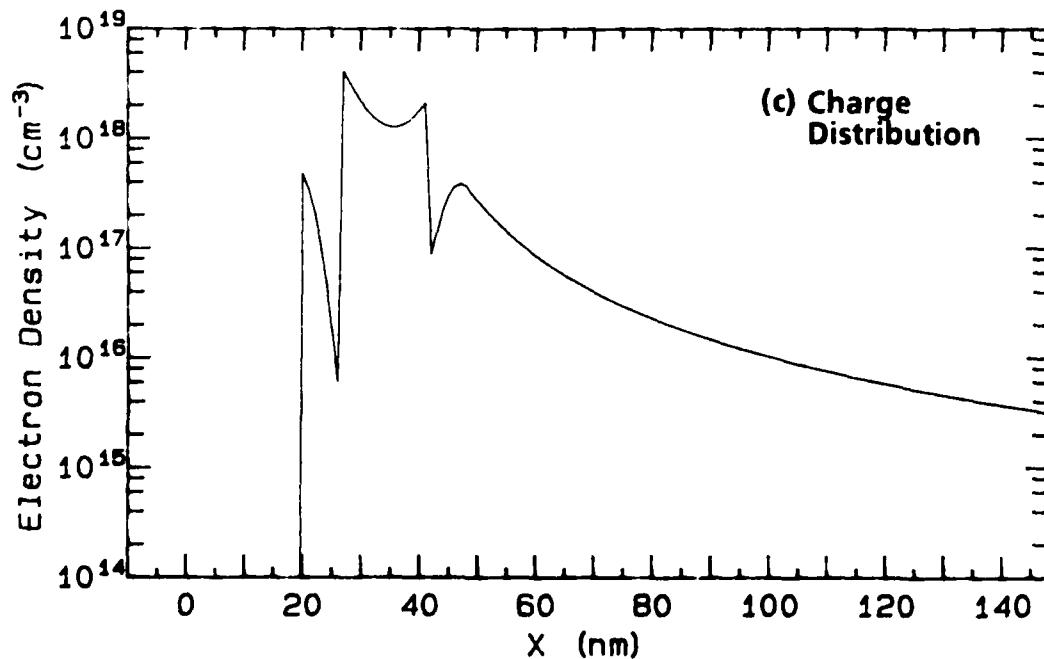
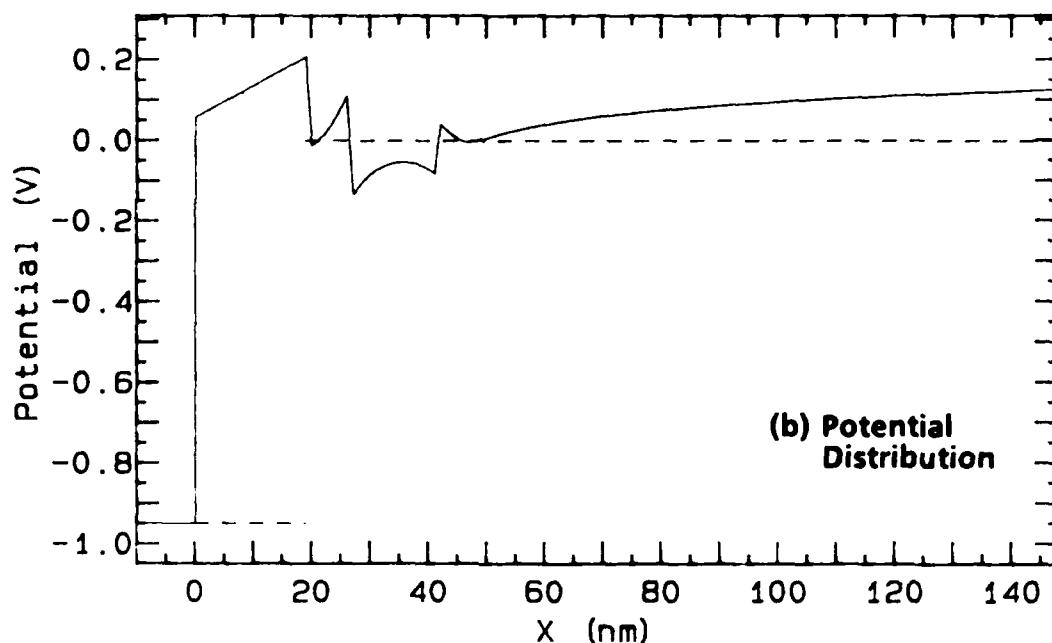
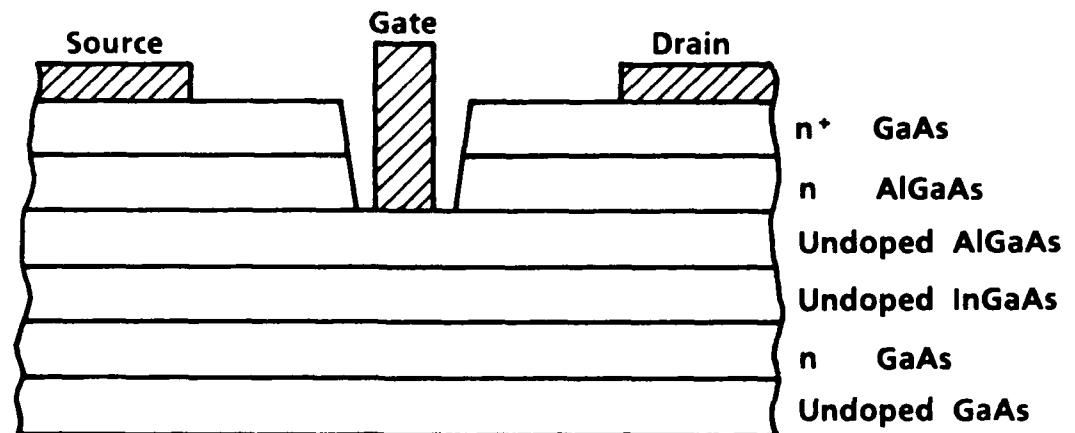


Figure 4. Quantum well MISFET with doped layer in both sides. (a) Material structure; (b) potential distribution; (c) charge distribution.

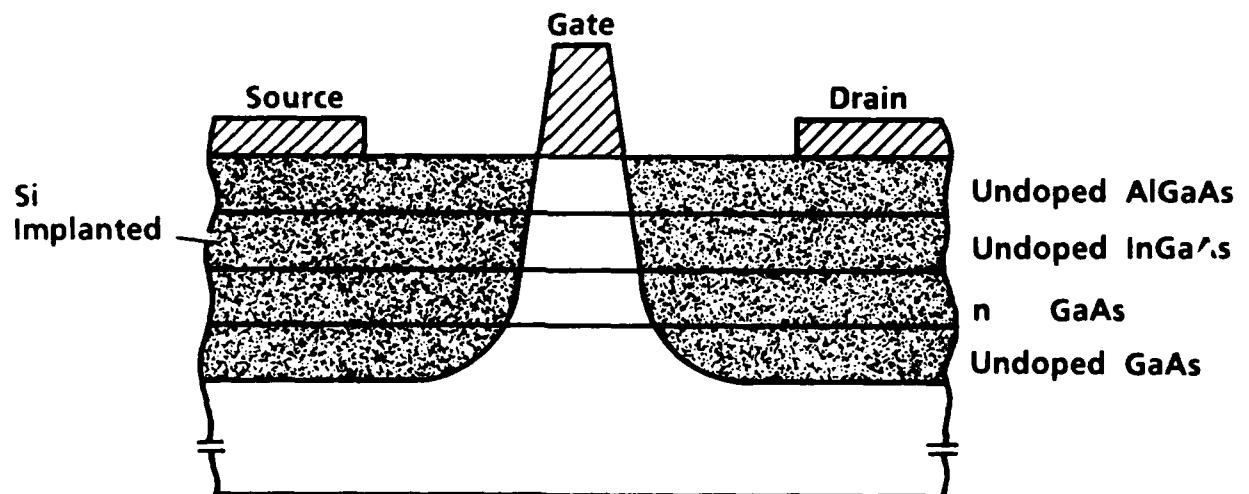
For power generation, a device should have a high gate-to-drain breakdown voltage. Breakdown usually occurs at the drain-side edge of a gate. Because of the large bandgap of the AlGaAs layer, the breakdown field of the MISFETs is extremely high. Breakdown occurs when the device is pinched-off, or nearly pinched-off, and the breakdown voltage is determined by the field generated by the residual positive charge at the doped layer. The doped layer is located far from the gate (except the structure in Figure 4), and a larger voltage can be applied for a given breakdown field. Moreover, there is a large charge accumulation (up to 72%) that does not contribute to the breakdown. Therefore, the breakdown voltage of this structure should be very high. In this structure the breakdown region may be the InGaAs layer because of the low breakdown field of the material, rather than the top layer, as is normal. If that is the case, we may introduce a doped layer as shown in Figure 4 without degrading the breakdown voltage.

The channels between the gate and the ohmic contacts (source or drain) should be able to handle an amount of current comparable to or more than the current under the gate when it is fully forward-biased. Otherwise, the accumulation charge cannot be utilized because of the series resistances. To prevent this problem, either self-aligned implantation techniques or other doped cap layers are needed. Figure 5 shows the device structures. In Figure 5(a) n⁺ GaAs and n-AlGaAs cap layers are added. In Figure 6 the carrier density with the cap layers has been calculated with the gate bias voltage of zero V (assuming that the Schottky barrier height is the same as the surface potential). The channel structure is identical to the Figure 1(a) structure. As shown, the well with the cap layers can carry charge comparable to that under the gate at forward bias. Figure 5(b) shows the implanted structure without the top layer. In this structure the charge in the channel is provided through the implanted multiple layers, and the AlGaAs layer may be depleted. Further improvement is expected by implanting the Figure 5(a) structure as it is in Figure 5(b).

The sheet carrier density of a MISFET can be increased by doping the active layer. The pseudomorphic MISFET shown in Figure 7 is easier to build than the quantum well MISFETs because the active layer is doped, which aids the ohmic contact process, and the material structure is simpler, which



(a)



(b)

Figure 5. Device structure of the quantum well MISFET. (a) Quantum well MISFET with doped cap layers; (b) quantum well MISFET with a self-aligned gate.

(a) Material Structure

Thickness	Composition	Doping	Electron Density
50 nm	GaAs	$3.0 \times 10^{18} \text{ cm}^{-3}$	$1.16 \times 10^{13} \text{ cm}^{-2}$
30 nm	$\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$	$3.0 \times 10^{18} \text{ cm}^{-3}$	$6.13 \times 10^{12} \text{ cm}^{-2}$
20 nm	$\text{Al}_{0.40}\text{Ga}_{0.60}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$1.35 \times 10^9 \text{ cm}^{-2}$
15 nm	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$2.06 \times 10^{12} \text{ cm}^{-2}$
2nm	GaAs	$1.0 \times 10^{10} \text{ cm}^{-3}$	$2.00 \times 10^{10} \text{ cm}^{-2}$
5 nm	GaAs	$3.0 \times 10^{18} \text{ cm}^{-3}$	$1.53 \times 10^{11} \text{ cm}^{-2}$
100 nm	GaAs	$1.0 \times 10^{13} \text{ cm}^{-3}$	$3.31 \times 10^{11} \text{ cm}^{-2}$

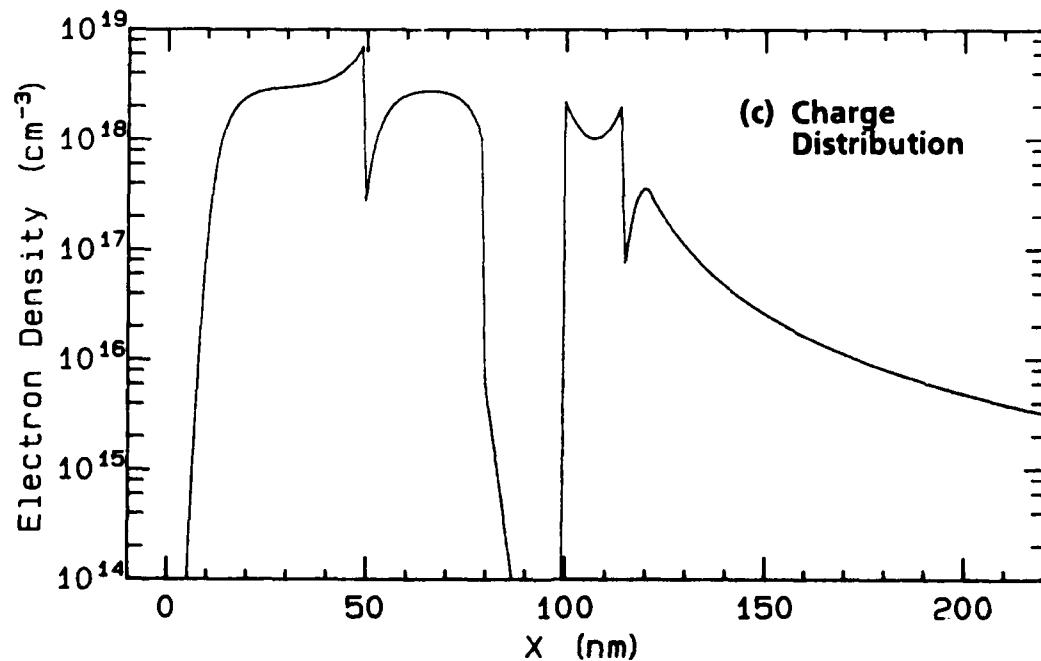
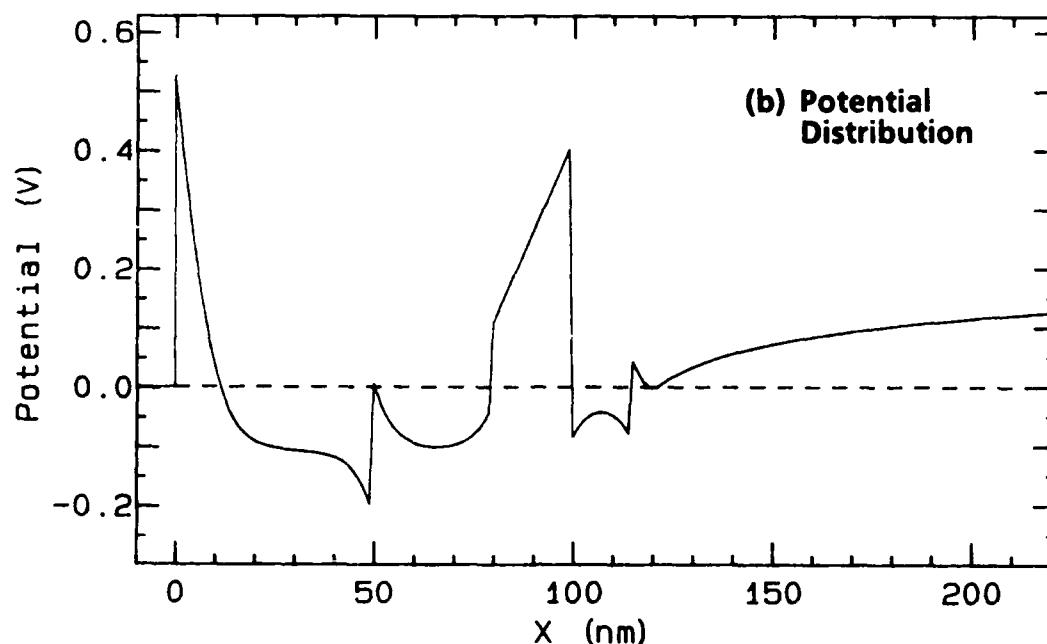


Figure 6. Channel carrier density of the quantum well MISFET with doped cap layers. (a) Material structure; (b) potential distribution; (c) charge distribution.

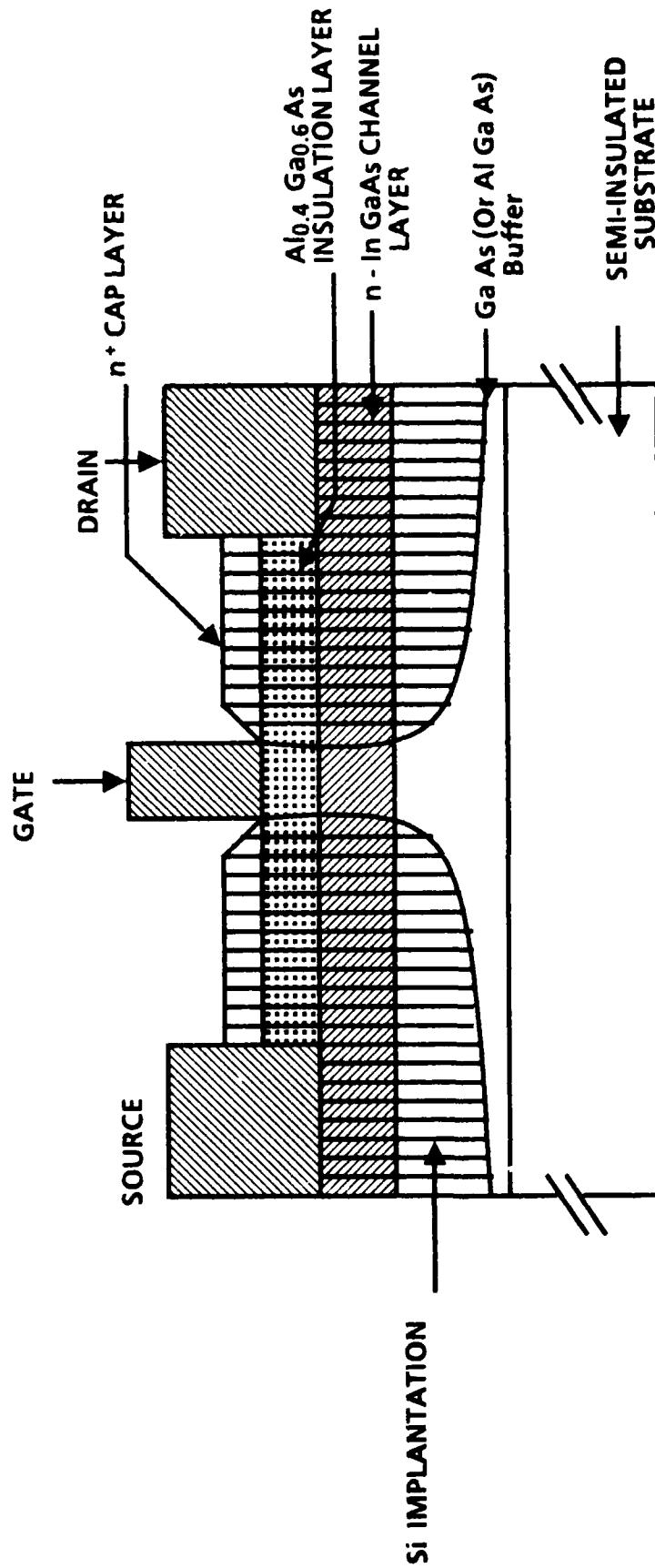


Figure 7. Pseudomorphic MISFET device.

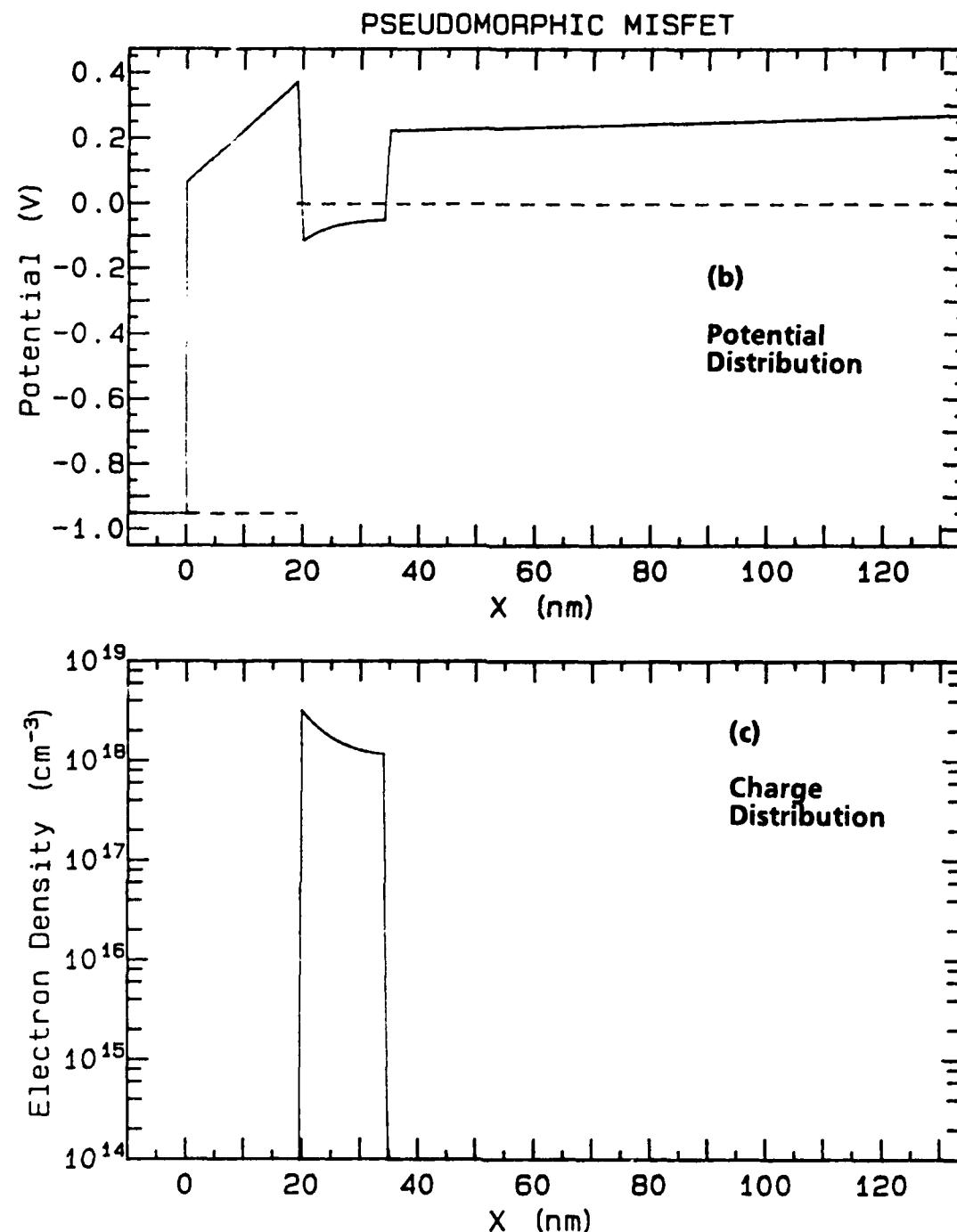
aids material growth. As shown below, this structure can accumulate more charge than the quantum well MISFETs. There are some trade-offs, however. The doped layer is closer to the surface, and the breakdown voltage may be lower. The carriers are moving through the heavily doped layer, which is a potential disadvantage. However, for a short gate FET, the degradation in f_t of a doped channel FET is minimal (see Section V).

Figure 8 shows the potential distribution and electron density profile of the pseudomorphic MISFET. The layer thicknesses and doping levels are also included in the figure. The doped layer sheet carrier density was $1.5 \times 10^{12}/\text{cm}^2$. When the Schottky diode was biased close to the barrier height, this structure accumulated charge in the well with a sheet carrier density of $1.11 \times 10^{12}/\text{cm}^2$ (74% of the doped density). The total sheet carrier density in the well increased to $2.61 \times 10^{12}/\text{cm}^2$. When the doping level of the layer was reduced, the accumulated charge density remained the same. Table 2 summarizes the calculated data. It is seen that high carrier density with large accumulation can be achieved in this structure.

Table 2
Sheet Carrier Density in the Well with Different Doping Levels

Doping Level (cm^3)	Doped Sheet Carrier (cm^2)	Accumulated Charge (cm^2)	Total Charge (cm^2)
1×10^{18}	1.5	1.11	2.61
7.5×10^{17}	1.125	1.14	2.26
5×10^{17}	0.75	1.17	1.92

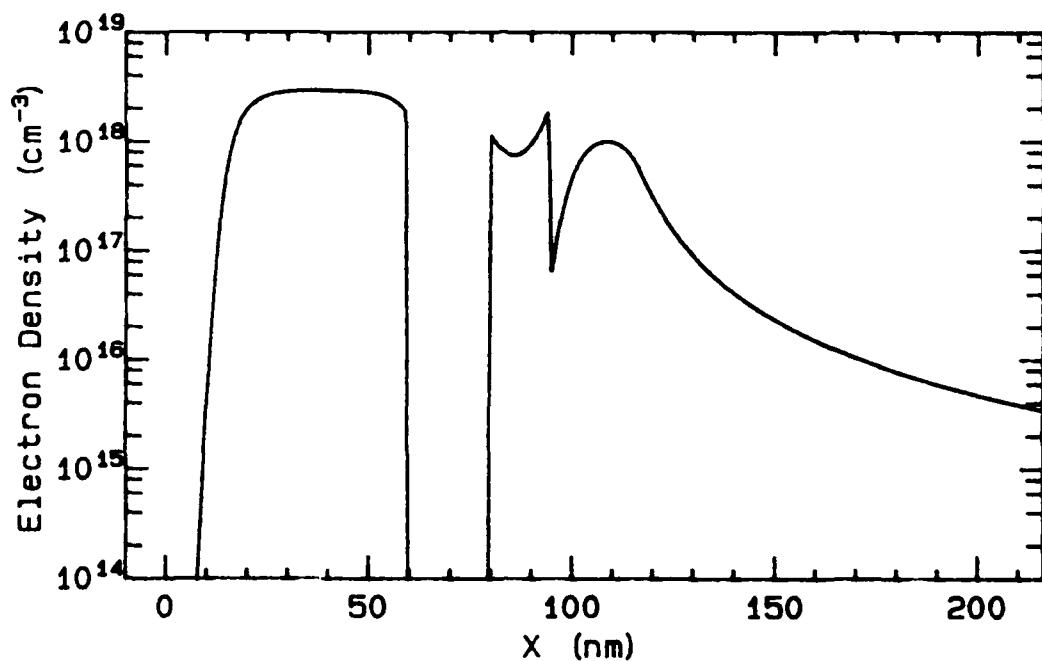
The computer program has been extended to predict the electron density profile measured using a C-V profiler. The profile obtained with the C-V profiler is different from the real profile because of inhomogeneous material structures, such as the heterointerface, and nonuniform doping. The program is very useful for evaluating the material structure of grown layers. Figure 9 shows the electron density profiles of two quantum well MISFETs (a normal structure and an inverted structure), as-grown. Figure 10 shows the



(a) Material Structure

Thickness	Composition	Doping	Electron Density
20 nm	$\text{Al}_{0.40}\text{Ga}_{0.60}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$3.38 \times 10^4 \text{ cm}^{-2}$
15 nm	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{18} \text{ cm}^{-3}$	$2.61 \times 10^{12} \text{ cm}^{-2}$
100 nm	$\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{13} \text{ cm}^{-3}$	$3.47 \times 10^8 \text{ cm}^{-2}$

Figure 8. Pseudomorphic MISFET. (a) Material structure; (b) potential distribution; (c) charge distribution.

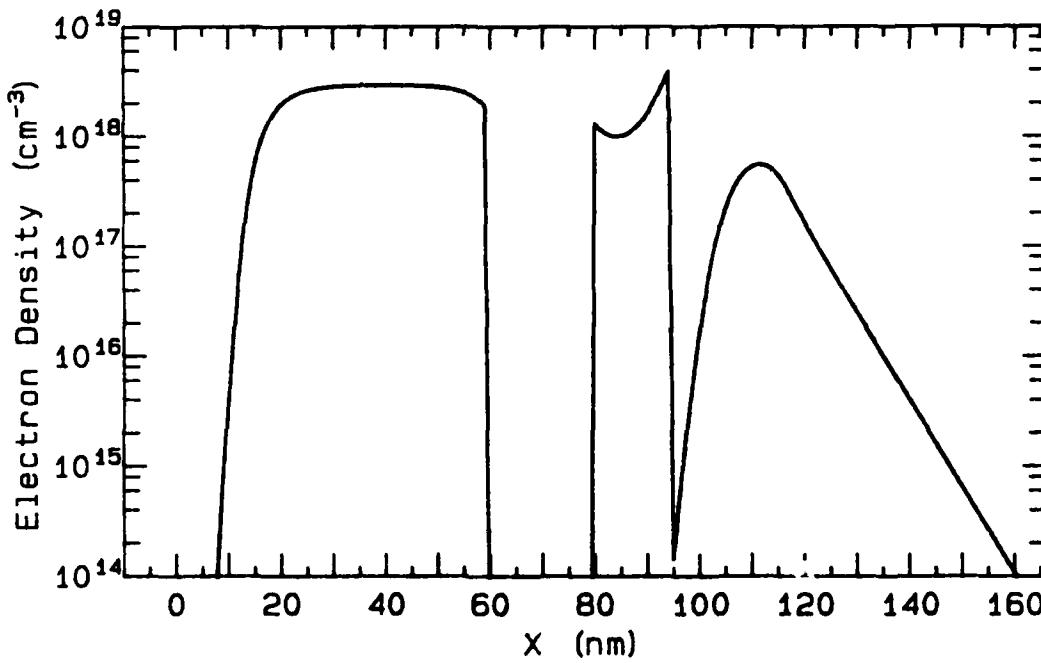


Temperature = 300 K
 Schottky barrier = 0.8 eV

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Thickness	Composition	Doping	Electron Density
60 nm	GaAs	$3.0 \times 10^{18} \text{ cm}^{-3}$	$1.16 \times 10^{13} \text{ cm}^{-2}$
20 nm	$\text{Al}_{0.40}\text{Ga}_{0.60}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$1.60 \times 10^6 \text{ cm}^{-2}$
15 nm	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{10} \text{ cm}^{-3}$	$1.54 \times 10^{12} \text{ cm}^{-2}$
2 nm	GaAs	$1.0 \times 10^{10} \text{ cm}^{-3}$	$1.76 \times 10^{10} \text{ cm}^{-2}$
20 nm	GaAs	$1.5 \times 10^{18} \text{ cm}^{-3}$	$1.50 \times 10^{12} \text{ cm}^{-2}$
100 nm	GaAs	$1.0 \times 10^{14} \text{ cm}^{-9}$	$1.66 \times 10^{11} \text{ cm}^{-2}$

Figure 9. (a) Electron density profiles - normal structure quantum well MISFET.



Temperature = 300 K
 Schottky barrier = 0.8 eV

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 10: 57

Thickness	Composition	Doping	Electron Density
60 nm	GaAs	$3.0 \times 10^{18} \text{ cm}^{-3}$	$1.16 \times 10^{13} \text{ cm}^{-2}$
20 nm	$\text{Al}_{0.40}\text{Ga}_{0.60}\text{As}$	$1.0 \times 10^{13} \text{ cm}^{-3}$	$1.75 \times 10^6 \text{ cm}^{-2}$
15 nm	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	$1.0 \times 10^{13} \text{ cm}^{-3}$	$2.46 \times 10^{12} \text{ cm}^{-2}$
2 nm	$\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$	$1.0 \times 10^{13} \text{ cm}^{-3}$	$5.60 \times 10^7 \text{ cm}^{-2}$
20 nm	$\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$	$1.5 \times 10^{18} \text{ cm}^{-3}$	$5.76 \times 10^{11} \text{ cm}^{-2}$
100 nm	$\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$	$1.0 \times 10^{13} \text{ cm}^{-3}$	$1.76 \times 10^{11} \text{ cm}^{-2}$

Figure 9. (b) Electron density profiles - inverted structure quantum well MISFET.

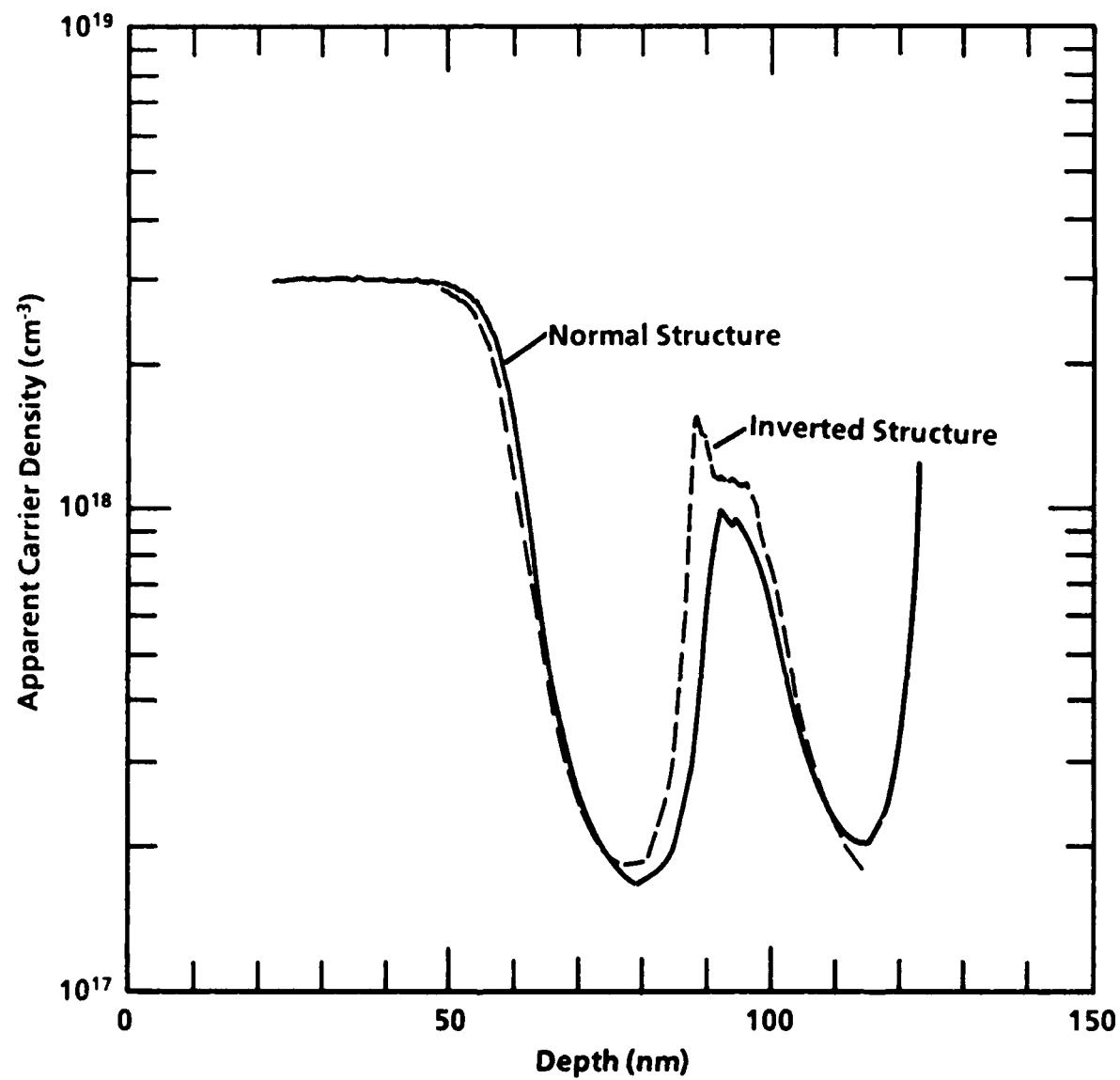


Figure 10. Calculated electron density profiles for C-V profiler measurement.

calculated electron density profiles expected from the C-V profiler for the two quantum well structures described in Figure 9. Figure 11 shows the measured profile of a normal structure quantum well MISFET [designed for the layer structure of Figure 9(a)]. The measured profile follows the calculated profile reasonably well, except in the doped region. In this sample the doping level in the bottom GaAs layer was too high, so the charge was not completely transferred to the InGaAs layer and formed two peaks. The C-V profiler and our calculations both predict a low $10^{17}/\text{cm}^3$ doping level for the undoped AlGaAs layer.

Doping Profile
Sample- MBE 1610, QW MISFET #3 Aug. 26, 1987 Frequency - 1×10^6 Hz
0.8V to -2V Sweep

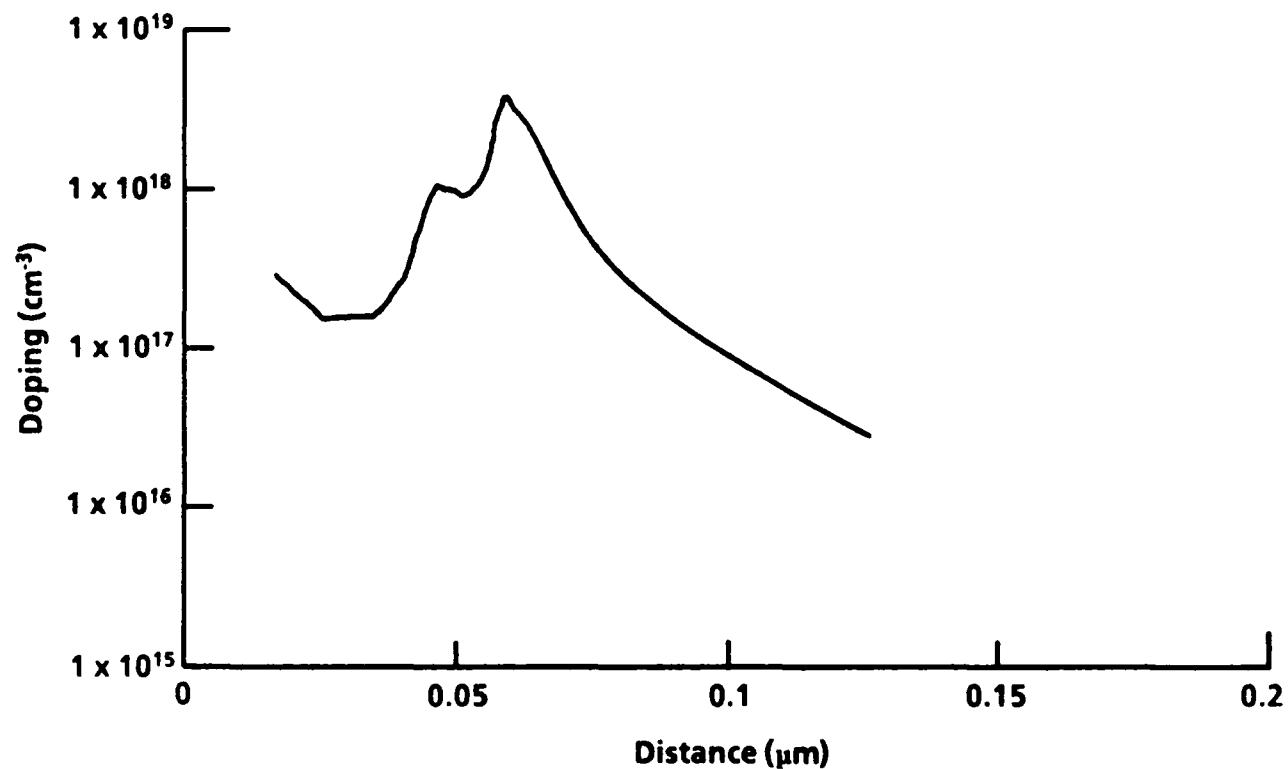


Figure 11. Measured electron density profile of the normal structure quantum well MISFET.

SECTION III

MATERIAL GROWTH

For growth condition optimization we have grown and evaluated a series of pseudomorphic HEMT materials using MBE. Table 3 shows the sheet carrier densities and mobilities of these materials at room temperature and at 77 K. As shown, we have achieved sheet carrier densities of about $2 \times 10^{12}/\text{cm}^2$ ($1.5 \times 10^{12}/\text{cm}^2$) with mobility of 5,000 (35,000) at room temperature (at 77 K), which is quite acceptable.

Table 3
Mobility and Sheet Carrier Density of Pseudomorphic HEMT Materials

Slice No.	Mobility (300 K)	Sheet Carrier Density (300 K)	Mobility (77 K)	Sheet Carrier Density (77 K)
1472	5200	2.69×10^{12}	31800	1.56×10^{12}
1473	5050	3.0×10^{12}	32600	1.66×10^{12}
1479	5260	2.69×10^{12}	33000	1.47×10^{12}
1480	4800	1.8×10^{12}	35600	1.27×10^{12}
1493	5370	2.9×10^{12}	35600	1.59×10^{12}
1494	4670	1.74×10^{12}	37600	0.8×10^{12}
1495	5440	2.36×10^{12}	39400	1.29×10^{12}

A $0.25 \times 75 \mu\text{m}$ gate HEMT has been built on this material and rf-tested. Figure 12 shows the I-V characteristics of the device. The measured extrinsic transconductance is 440 mS/mm. The material structure is shown in Figure 13. To simplify the material evaluation, the n^+ contact layer was omitted from this material, which will degrade device performance. However, the device performance was acceptable. At 31 GHz a power-added efficiency of 37% was obtained at a power density of 0.53 W/mm and 5 dB gain. When the device was optimized for higher output power, the power density was 0.7 W/mm at a power-added efficiency of 27% and 3.7 dB gain. At 59 GHz a power-added efficiency of 20.7% was achieved at a power density of 0.3 W/mm and 3.3 dB gain. The device also had a good noise figure. At 18 GHz the noise figure

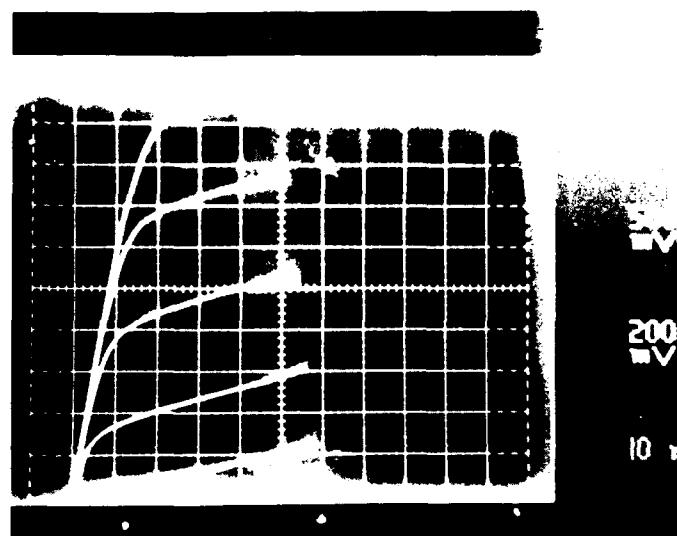


Figure 12. I-V characteristics of a $75 \mu\text{m} \times 0.25 \mu\text{m}$ InGaAs pseudomorphic MODFET ($g_m = 440 \text{ mS/mm}$).

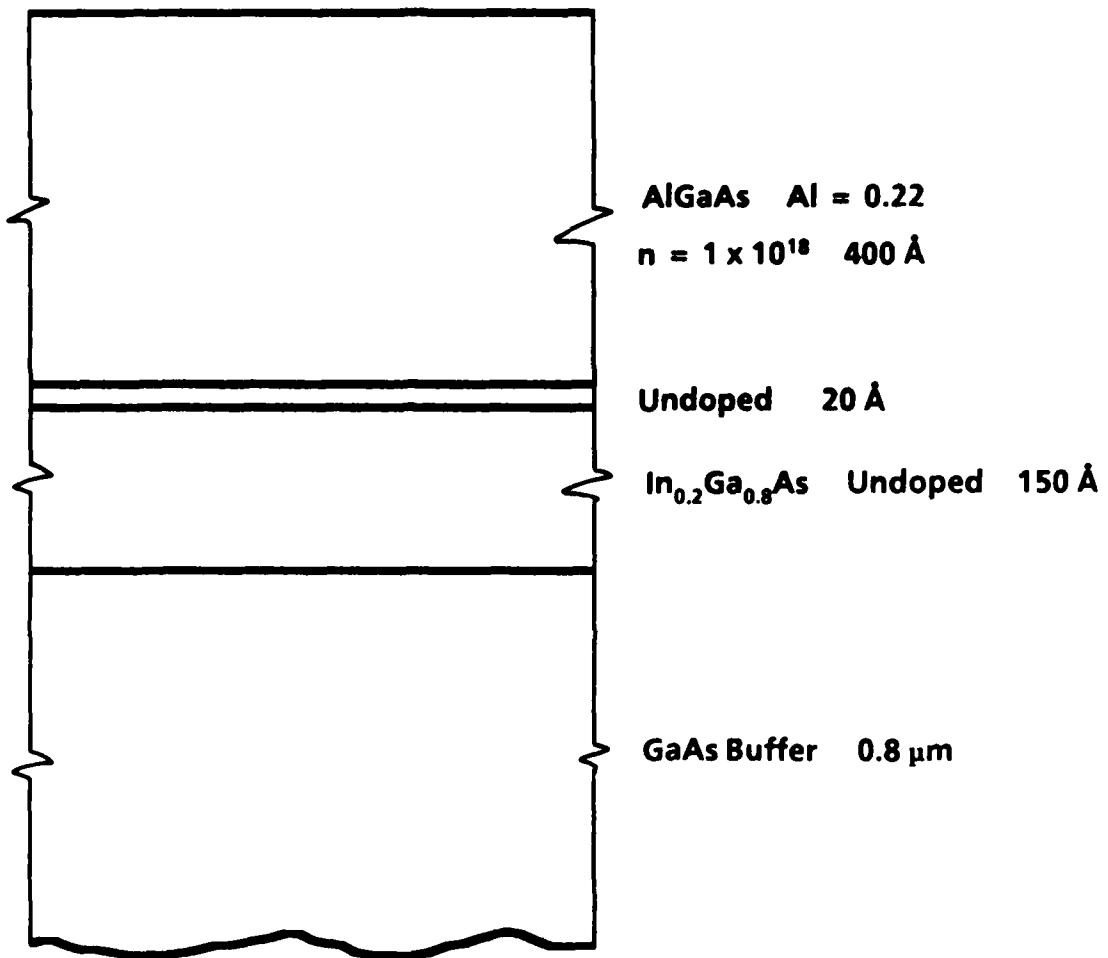
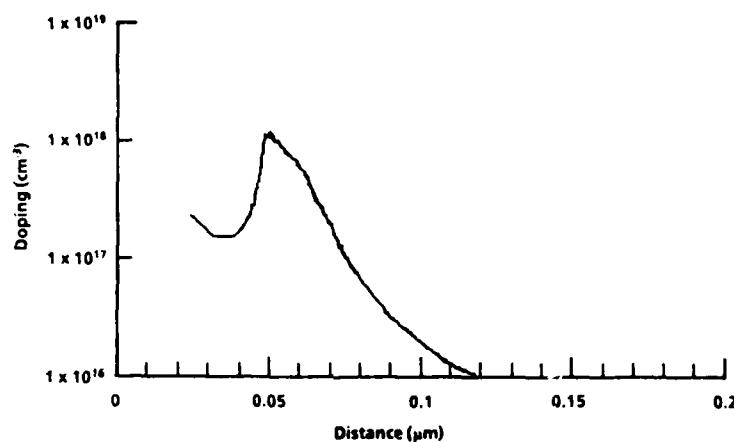


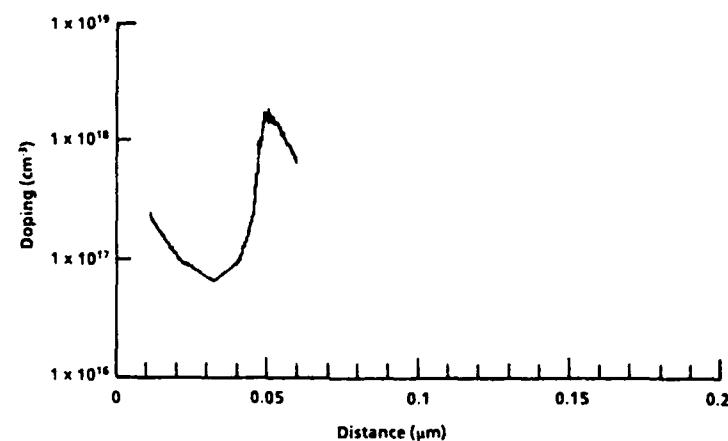
Figure 13. Pseudomorphic MODFET structure.

was 0.92 dB with 11.6 dB associated gain. These results clearly show that our pseudomorphic material quality is state of the art.

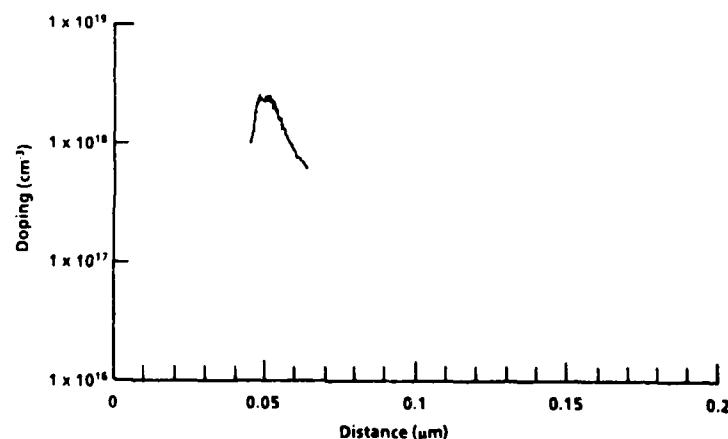
Further efforts have been made to optimize the growth conditions of the quantum well MISFETs. We have grown series of slices (normal structure) with the n-type GaAs layer doped to $2.5 \times 10^{18}/\text{cm}^3$, $4.5 \times 10^{17}/\text{cm}^3$, and $6 \times 10^{18}/\text{cm}^3$. The layer thicknesses have been adjusted until all the charge has been transferred from the doped layer to the quantum well. This occurred at layer thicknesses of 50 Å, 30 Å, and 25 Å, respectively. The amount of charge in the well has been evaluated using the C-V profiler. As shown in Figure 14, the amount of charge continuously increased as the doping level increased. The peak doping levels in the well were $1.1 \times 10^{18}/\text{cm}^3$, $1.6 \times 10^{18}/\text{cm}^3$, and $2.4 \times 10^{18}/\text{cm}^3$, respectively. Apparently, the heavily doped layer favors a power MISFET. Having solved the material growth problem for the normal structure MISFET, we next initiated the material growth condition optimization for an inverted structure MISFET.



(a)



(b)



(c)

Figure 14. Doping profile of quantum well MISFET obtained from C-V profiler. (a) n-GaAs, $2.5 \times 10^{18}/\text{cm}^3$, 50 Å; (b) n-GaAs, $4.5 \times 10^{18}/\text{cm}^3$, 30 Å; (c) n-GaAs, $6 \times 10^{18}/\text{cm}^3$, 25 Å.

SECTION IV

PROCESS DEVELOPMENT

The parasitic resistances of the quantum well MISFET can be high; (1) ohmic contact through the multiple layer (including the undoped AlGaAs layer) will be difficult, and (2) the series resistances for the channels between the spacing of gate and ohmic contacts are high. For proper operation of the quantum well MISFETs at millimeter-wave frequencies, therefore, we developed the processes necessary to minimize the parasitics.

Ohmic contacts have been made using the three methods shown in Figure 15. In the first process, ohmic metal was alloyed through the multiple layers described in Figure 8. The standard MESFET process was used. the contact resistance was 2.1×10^{-5} ohm-cm 2 . As shown in Figure 15, the alloy can be applied directly when the AlGaAs layer thickness is 100 Å or less; however, a layer thickness of more than 200 Å is necessary to prevent excessive gate leakage current, so the first method could not be applied. In the second method, the undoped AlGaAs layer was etched away, and ohmic contact was made on the n-GaAs layer. The specific contact resistances were in an acceptable range when we used the second approach (mid 10^{-6} ohm-cm 2). However, the second method has a repeatability problem caused by selective etching of the AlGaAs layer and by the channel resistance of the small gap between the ohmic metal and the unetched region.

We have investigated a new ohmic contact metal system for the first process. The MISFET structure, consisting of 600 Å of n⁺ GaAs on top, then 200 Å of undoped Al_{0.4}Ga_{0.6}As, and 200 Å of n-GaAs, was used as a test sample. The metal system consists of 100 Å Ni/1500 Å AuGe/300 Å Ag/1000 Å Au. In a series of experiments pieces of the slice were alloyed using a rapid thermal anneal at temperatures from 425°C to 525°C (every 25°C step) for 10 and 20 seconds. We obtained the best results with a 20-second anneal at 475°C. Specific contact resistance was around 4×10^{-7} ohm-cm 2 , which is very good, considering the contact through the undoped AlGaAs layer.

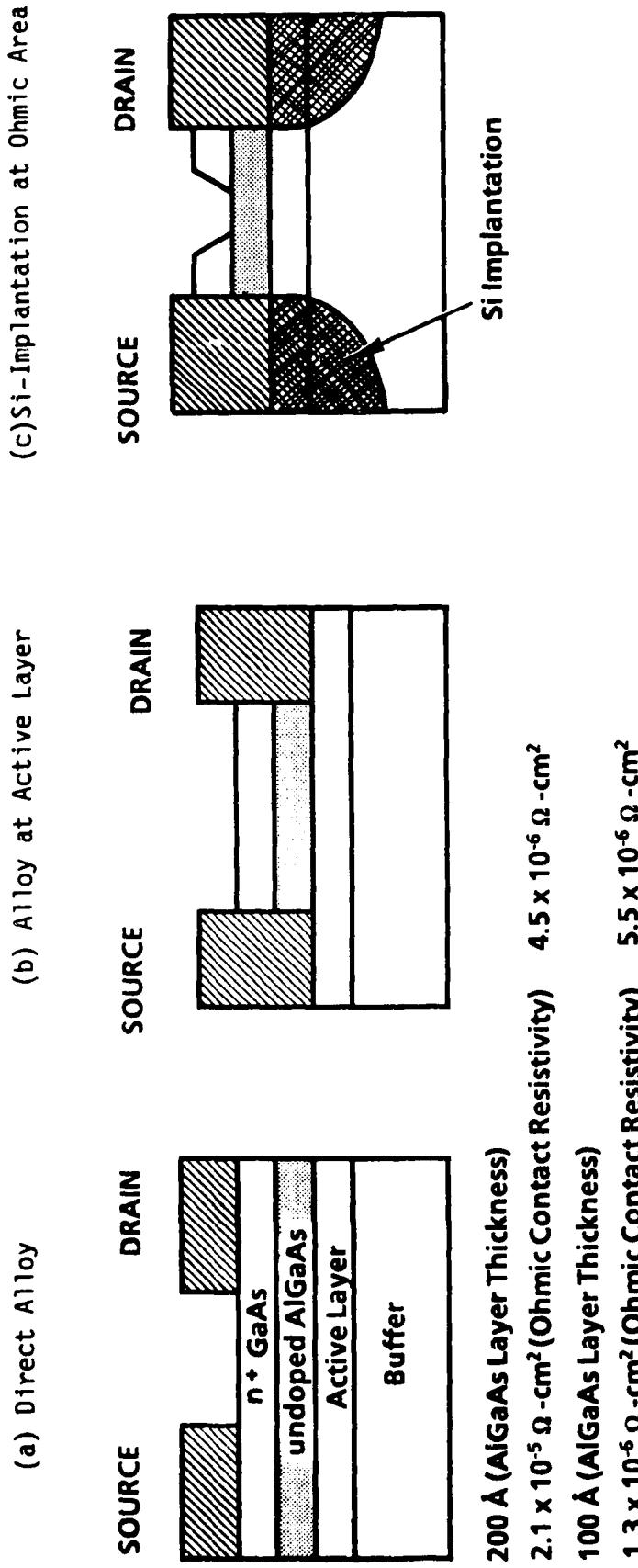


Figure 15. Ohmic contact process (pseudomorphic MISFET).

We have investigated a similar ohmic contact metal system for the quantum well MISFETs. The metal system consists of 200 Å Ni/1500 Å AuGe/200 Å Ni/1000 Å Ag/1000 Å Au. Pieces of the slice were alloyed using a rapid thermal anneal at temperatures from 425°C to 550°C (every 25°C) for 15 seconds. We obtained the best results with a 15-second anneal at 525°C. Ohmic contact resistance was around 0.14 ohm-mm, which is acceptable.

For a better contact, n⁺ implantation at the contact area is required (the third method). For that purpose, Si implantation and activation experiments have been performed to establish the optimum procedure. The focus has been on determining the shortest annealing time that will adequately activate an n⁺ implant, while minimizing Si diffusion through the layers. A rapid thermal anneal process is used. The initial tests have used semi-insulating GaAs substrates with a 500 Å CVD Si₃N₄ cap. Si²⁹ was implanted at 60 keV with a dose of $10 \times 10^{12}/\text{cm}^2$ and 180 keV with a dose of $60 \times 10^{12}/\text{cm}^2$. Figure 16 shows the results of one set of experiments where samples were annealed at 850°C, 950°C, and 1000°C. The one-second anneal at 1000°C was chosen for the next set of experiments because the conductivity of 11.7 mS/sq is sufficiently high for our purposes, and it will maintain the material structure intact because of the extremely short annealing time. Currently, we are optimizing the RTA process for the quantum well MISFET.

A self-aligned gate process has been developed to reduce the series resistances between the gate and ohmic contacts. From the many self-aligned gate processes, we selected the SAINT process. It is a substitutional gate process, as illustrated in Figure 17. Using photoresist/Ge/PMMA multilayer resist, a dummy gate was formed and used first as an implant mask, and then to lift off a dielectric layer. The implantation was given a rapid thermal anneal, and ohmic contacts were placed on the two implanted regions. The device process was completed by realigning the gate to the trough left in the dielectric. The advantage of this process over others is that there is no restriction on the metalization used for the gate.

For millimeter wave applications, the use of a gold-based gate is critical because of the gate resistance. Unlike many other technologies,

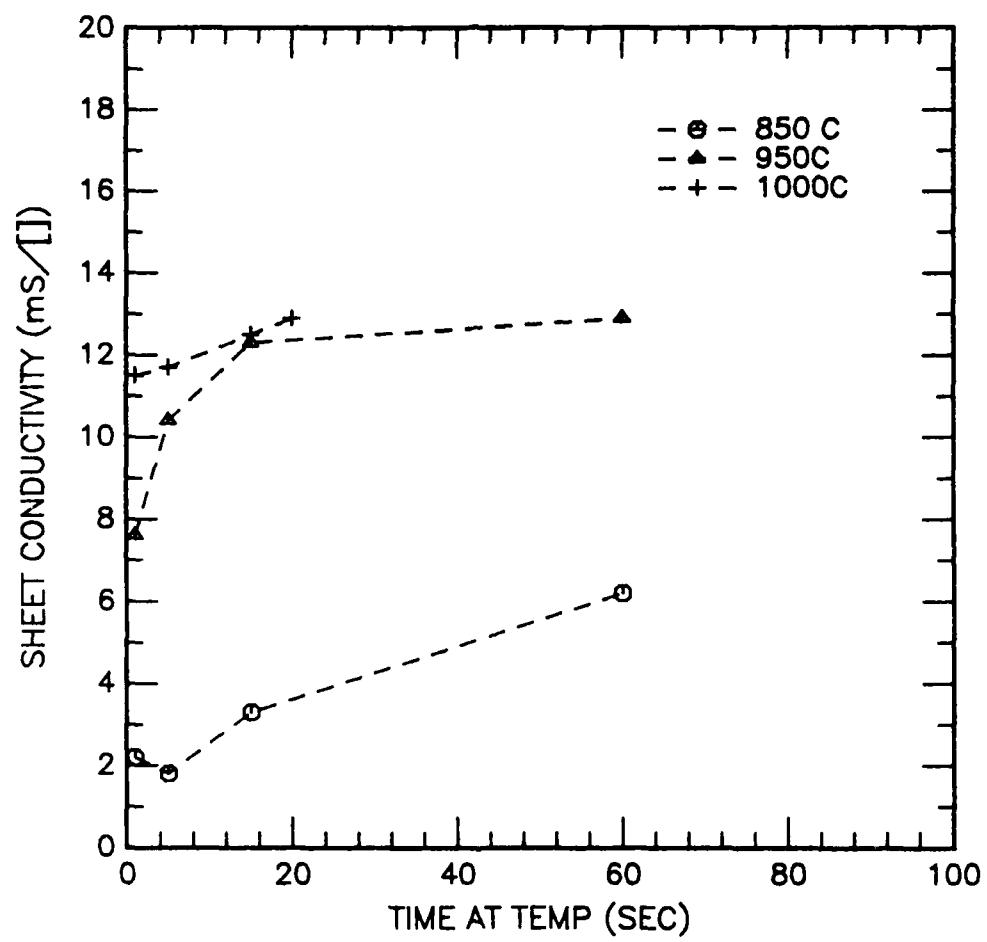


Figure 16. Rapid thermal annealing activation characteristics of implanted Si.

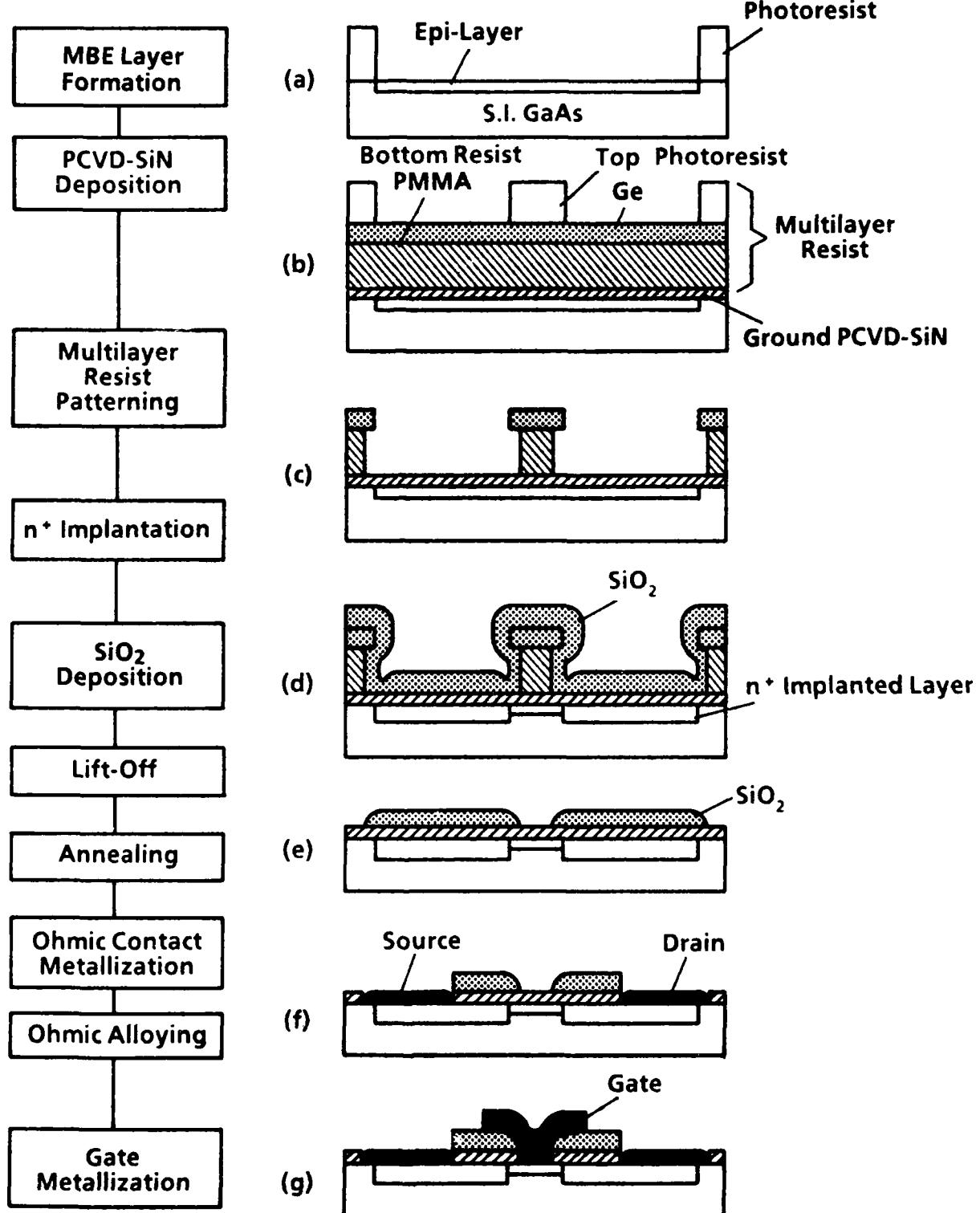


Figure 17. SAINT process sequence.

this process allows the gate region to be recessed, and it produces a gate with a T-shaped cross section. Figure 18(a) shows a $0.3 \mu\text{m}$ dummy gate that consists of PMMA and Ge. Figure 18(b) shows the dummy gate with a SiO_2 layer on it. Figure 18(c) shows the completed gate with a T-shaped cross section. Figure 19 shows the I-V curve of the completed device processes on a test sample (n-GaAs), indicating that it is operating properly. Currently, we can produce $0.25 \mu\text{m}$ gates with a high yield. We are optimizing the implantation and annealing process for the pseudomorphic structures.

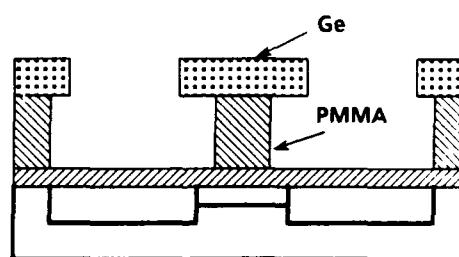
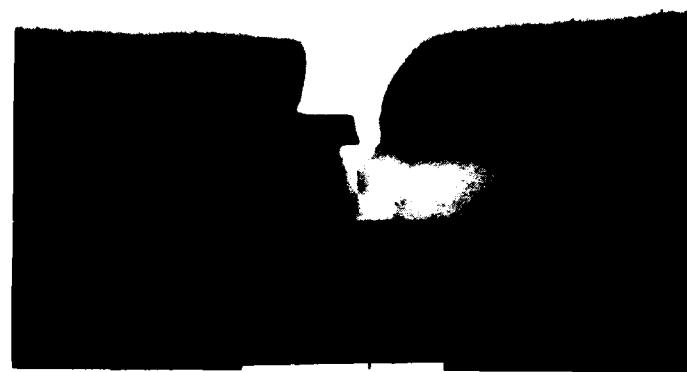


Figure 18. Saint process. (a) Dummy gate formation.

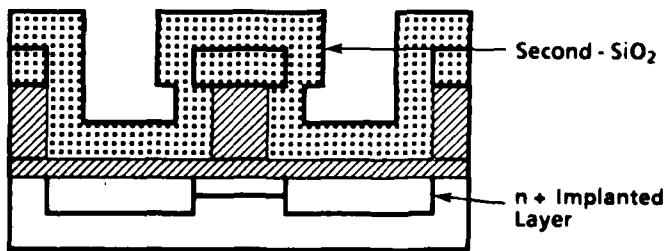
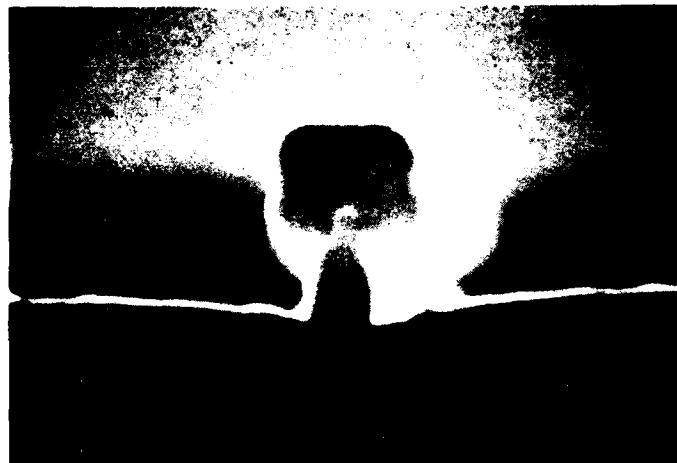


Figure 18. (Continued) (b) SiO_2 deposition.

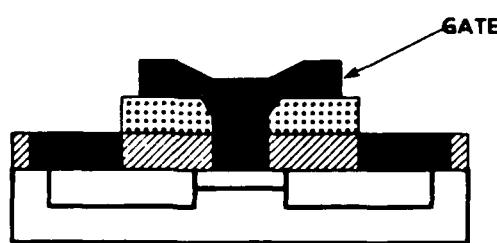
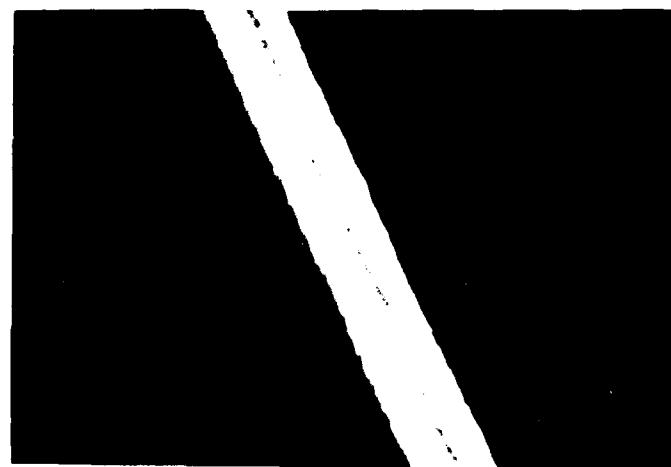


Figure 18. (Continued) (c) Gate deposition.

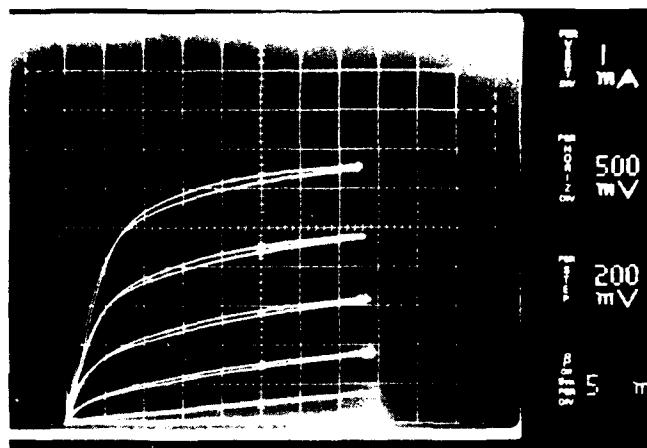


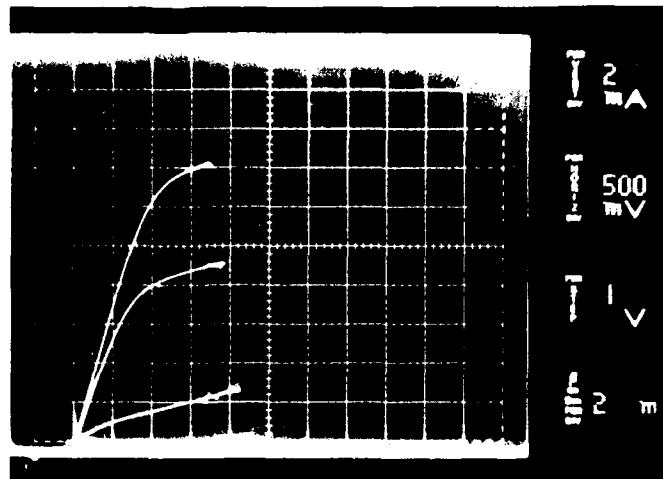
Figure 19. Drain current/voltage curve of a $75 \mu\text{m}$ FET with a SAINT-processed $0.3 \mu\text{m}$ gate.

SECTION V

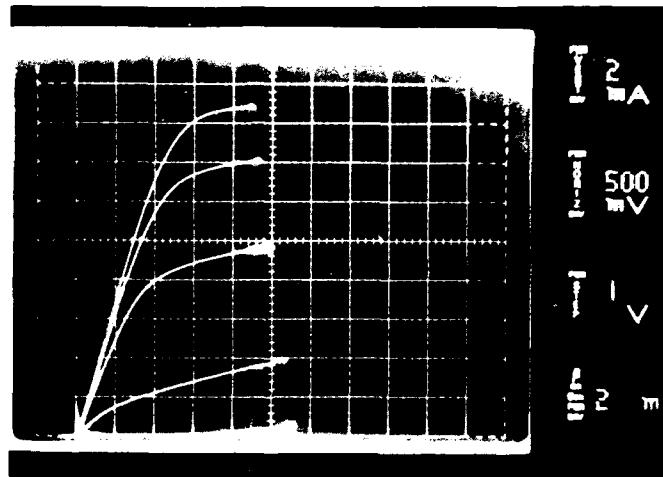
DEVICE PERFORMANCE

A $0.3 \times 75 \mu\text{m}$ normal structure quantum well MISFET was fabricated with the material structure of Figure 11. Its I-V curve is shown in Figure 20. It has a maximum transconductance of 260 mS/mm at a gate bias of -1.5 V . This device was non-self-aligned, and the transconductance was compressed when it was forward-biased because of the series resistance problem. Cap layers have been added for subsequent slices to get a working device without using the self-aligned technique, which is under process development. The material structures (two slices) and their carrier density profiles are shown in Figure 21. The first one (No. 1653) has electrons in the well and at the doped GaAs layer, while the second (No. 1676) has charge only in the well. We have built $0.25 \times 75 \mu\text{m}$ FETs on these materials. The f_t 's were 30 GHz and 50 GHz , respectively. The f_t of the first device is comparable to a MESFET, while that of the second device is comparable to a pseudomorphic HEMT. The input resistances were comparable to those of a HEMT, indicating that we have good ohmic contacts. The dc characteristics of the devices are shown in Figure 22. The maximum currents were 670 mA/mm and 540 mA/mm , respectively, and the transconductances 280 mS/mm and 330 mS/mm , respectively. The transconductances are quite uniform for the gate bias voltages. The gate-drain breakdown voltages were $10 \sim 13 \text{ V}$ with hard breakdown characteristics. The Schottky barrier heights were about 1.4 V . All these dc data indicate that we built properly working quantum well MISFETs, although the structures are not yet optimized.

The devices were tested at 60 GHz . Small signal gains were $4 \sim 6 \text{ dB}$ for both devices. For power tuning of the second device, linear gain was 3.2 dB , and it generated 0.3 W/mm at 1 dB compression (2.2 dB gain). The power gain of the first device was 1 dB lower. The first device was tested at a lower frequency (32 GHz). It had linear gain of 7.2 dB , and at 1 dB compression it generated a power density of 0.55 W/mm with 21% power-added efficiency. The saturated power density was 0.7 W/mm . The power saturation curve is shown in Figure 23. The gain of the second device was about 1 dB lower at this frequency. The better performance of the second device at the higher



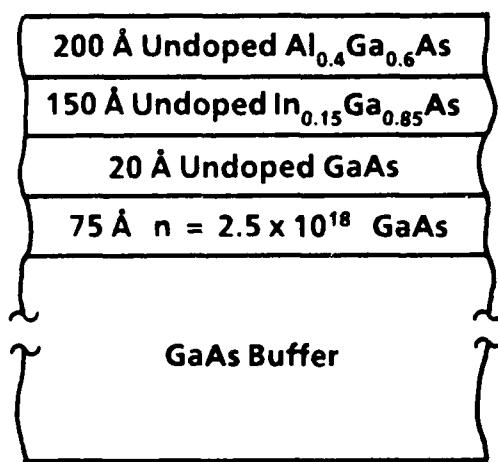
(a) $V_g = 0V$
on Top Line



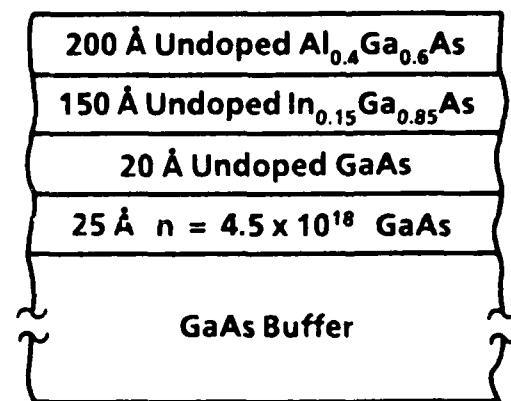
(b) $V_g = 1V$
on Top Line

Maximum $G_m = 260 \text{ mS/mm}$

Figure 20. I-V characteristics of quantum well MISFET.

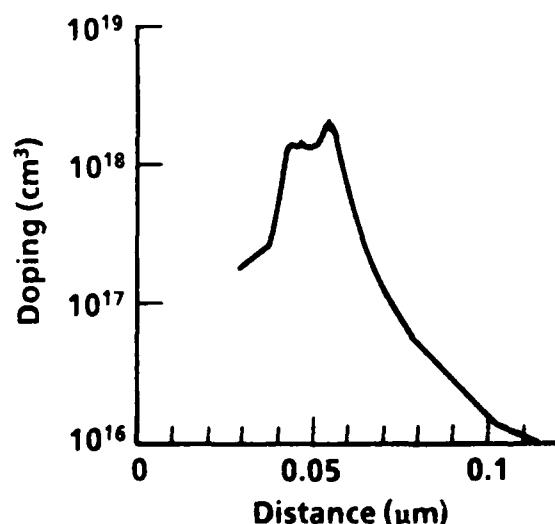


No. 1653

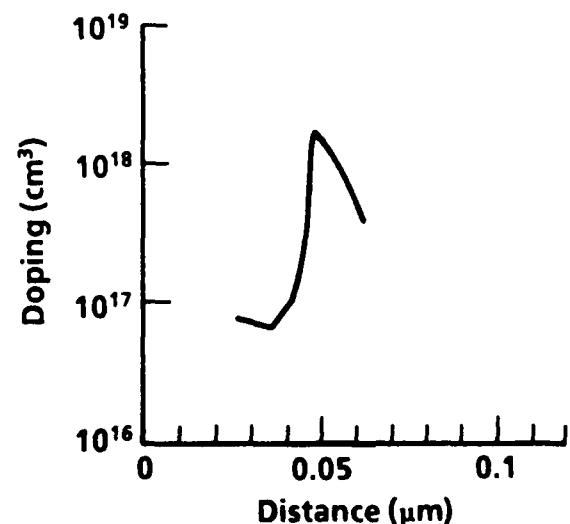


No. 1676

(a) Material Structures



No. 1653



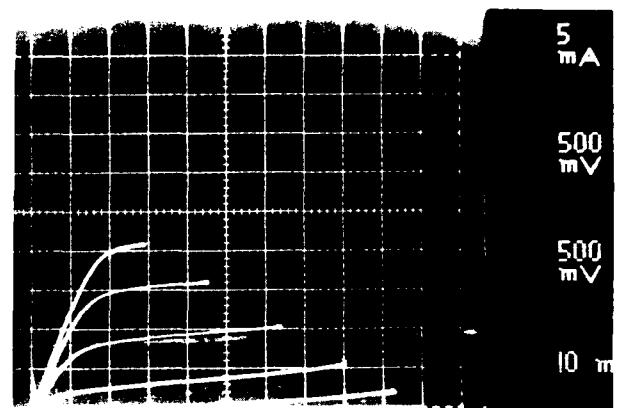
No. 1676

(b) Charge Carrier Profiles

Figure 21. Two quantum well MISFET materials. (a) Material structure; (b) charge carrier profiles.

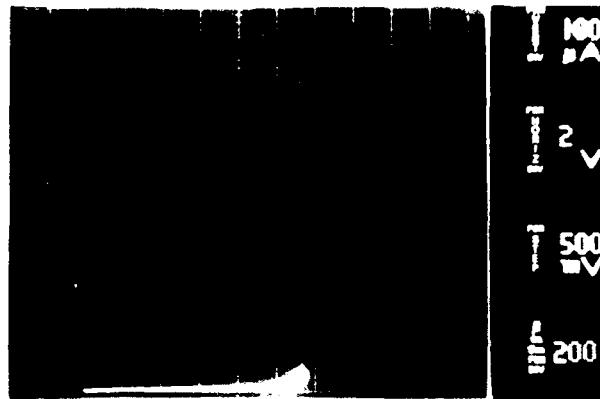


No. 1653

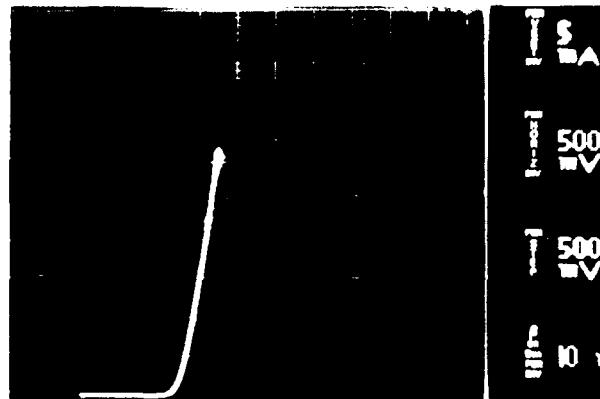


No. 1676

(a) I-V Curve



(b) Gate-Drain Breakdown Curve



(c) Gate Forward Characteristic

Figure 22. Dc characteristics of quantum well MISFETs. (a) I-V curve; (b) gate-drain breakdown curve; (c) gate forward characteristic.

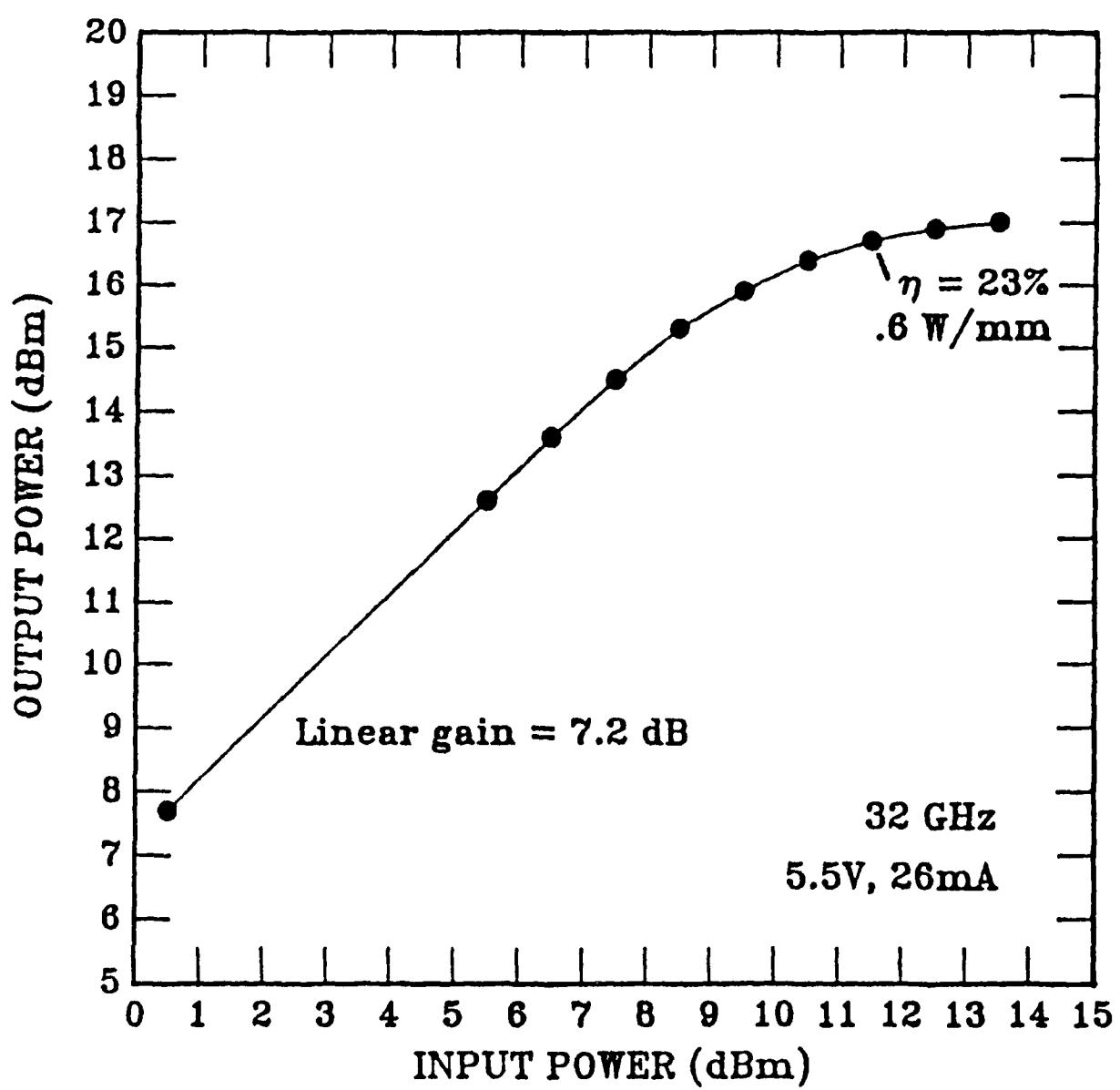


Figure 23. Power saturation curve of No. 1653 quantum well MISFET.

frequency may be related to the higher f_t (f_{max} was comparable). These data show that the quantum well MISFETs are capable of generating power, but the power gain is still low. To improve device performance further, the structure of quantum well MISFETs has been modified to increase the sheet carrier density in the well and the transconductance.

Under an AFWAL contract we are working on a modified version of the highly doped MISFET that we call the "InGaAs Pulse-Doped FET." The GaAs conductive layer is replaced by a highly doped layer of InGaAs. The introduction of In leads to better electron propagation properties. The material structure, shown in Figure 24, consists of a GaAs buffer, a thin layer (55 Å) of InGaAs, 1000 Å of GaAs doped $8 \times 10^{17}/\text{cm}^3$, and a 1000 Å top layer of n^+ GaAs. Only a 33 Å thick layer of InGaAs is doped, and it is separated from the GaAs by two 11 Å thick layers of undoped InGaAs on each side. Devices with 50 and 75 μm gate widths and 0.3 μm gate lengths have been fabricated on the material.

The 75 μm device has been tested at 60 GHz, and a small signal gain of 8 dB has been achieved. When tuned for high power, the device had 0.6 W/mm power density with 3.5 dB gain and 14% power-added efficiency. At 5.1 dB gain it delivered 0.4 W/mm power density with 13% efficiency. This is the highest power density ever achieved from a three-terminal device at this frequency. Figure 25 shows the gain compression curve of the InGaAs pulse-doped MESFET. S-parameter data indicate that the f_t of this device was comparable to that of a pseudomorphic HEMT (around 55 GHz).

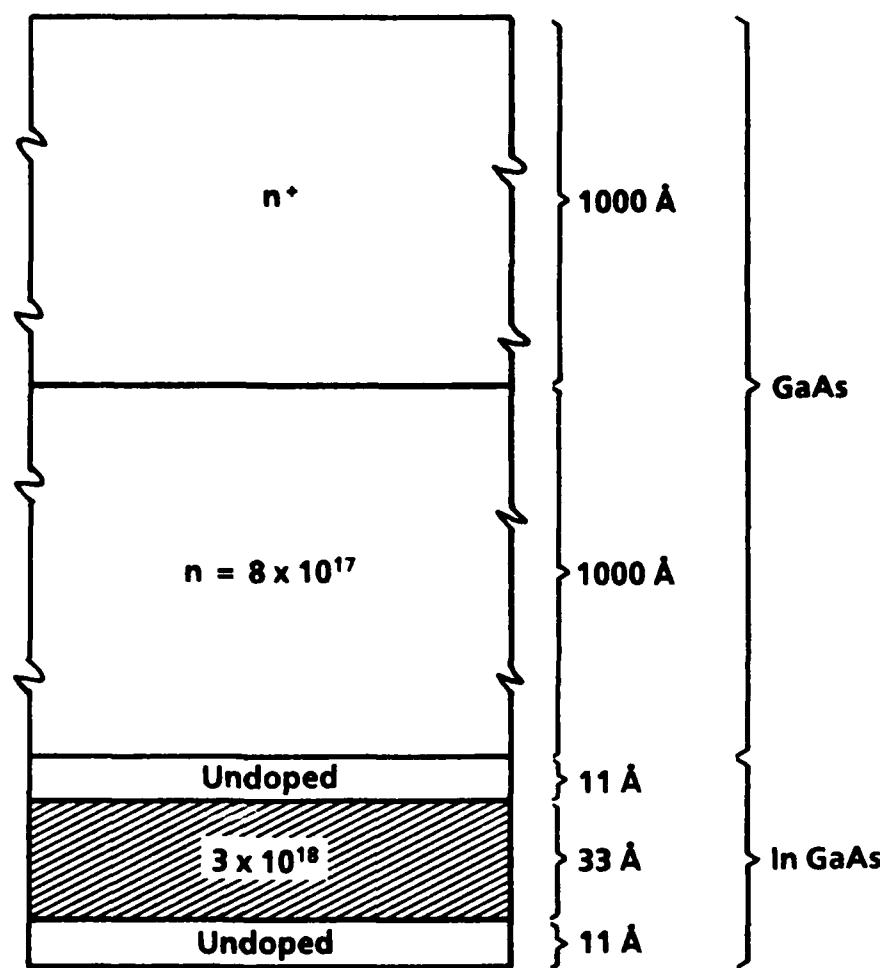


Figure 24. InGaAs pulse-doped material structure.

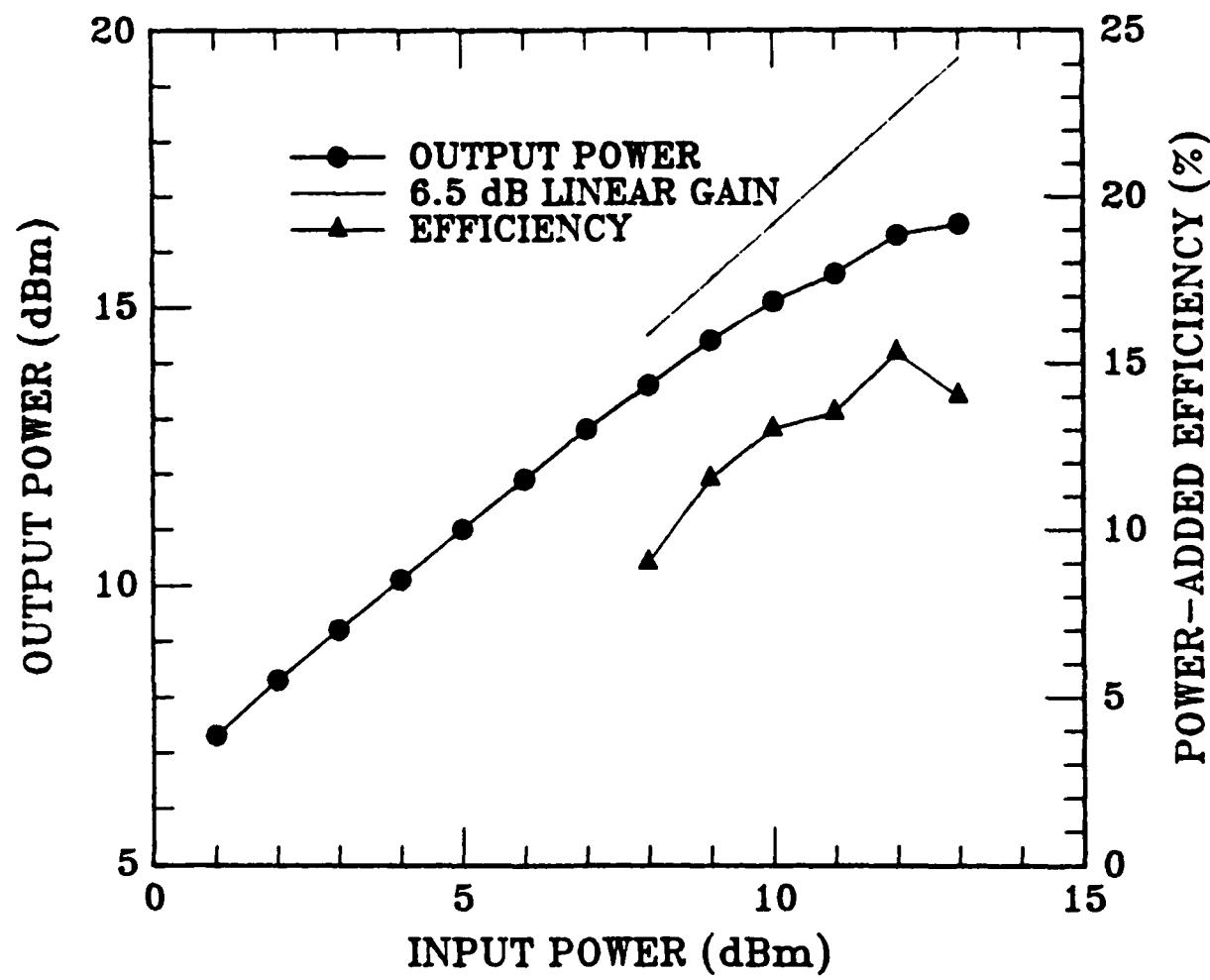


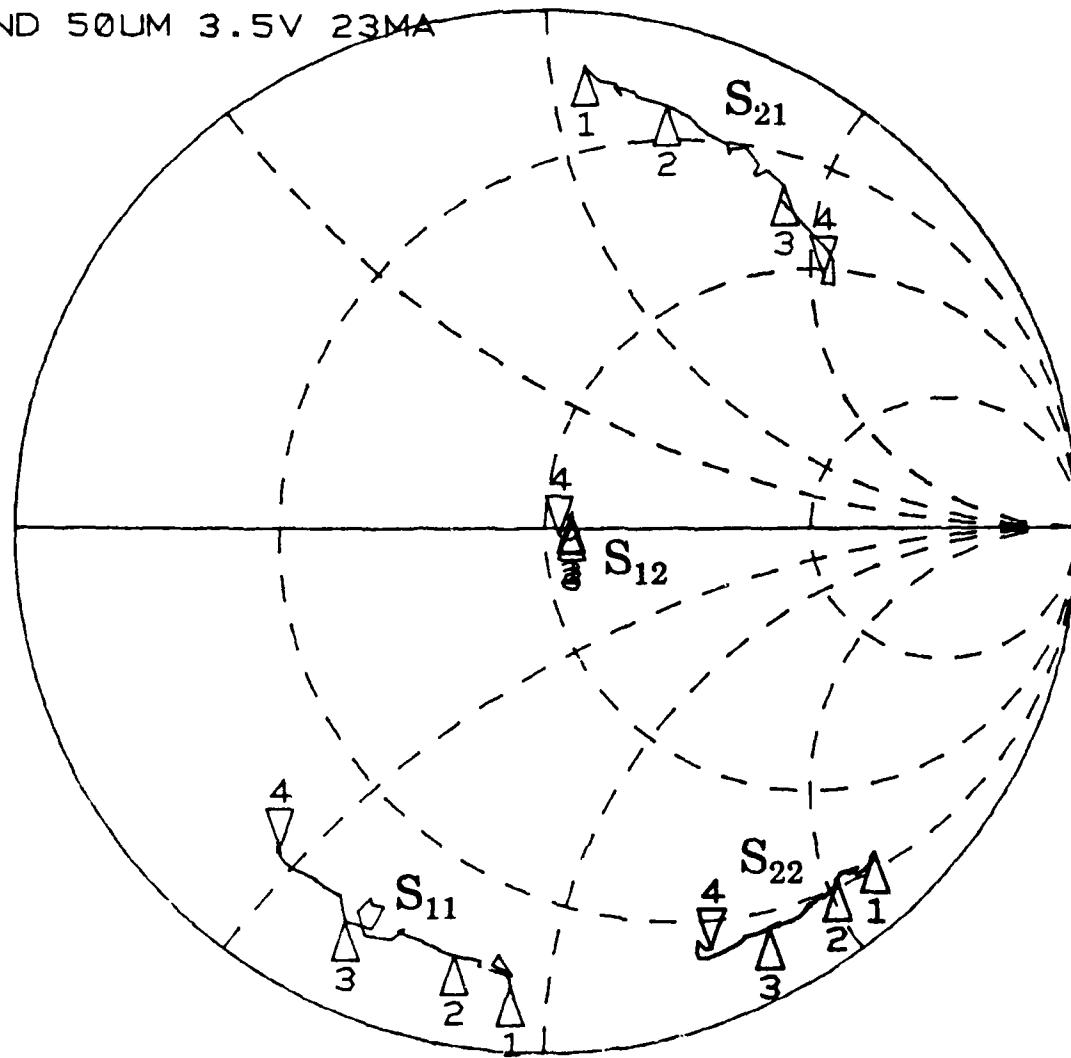
Figure 25. Gain compression curve of InGaAs pulse-doped MESFET at 60 GHz.

SECTION VI
MILLIMETER-WAVE S-PARAMETER MEASUREMENTS

Our S-parameter measurement capability has been extended to millimeter-wave frequencies under an AFWAL program. Using the HP 8510 and extender, we have successfully measured the parameters at the 26.5 to 40 GHz band and the 50 to 75 GHz band. For this measurement we used a 50 μm gate width FET intended for V-band operation. A finline-to-waveguide transition was used to interface the device with the waveguide measurement setup. A deembedding/calibration procedure that utilized the TSD (through-short-delay) method was used. The device was stabilized at low frequencies by providing resistive loading through the finline shorts. Figure 26 shows typical Smith chart plots of FETs at the frequencies. These plots show that the data were relatively smooth and corresponded with the lower frequency data. Figure 27 is a plot of the maximum available gain (as computed from the measured V-band S-parameters) as a function of frequency for a V-band FET. It clearly shows the expected 6 dB/octave gain roll-off. Our demonstrated millimeter-wave S-parameter measurement capability should greatly enhance the device modeling for the MISFET optimization and amplifier design of this program.

REF 1.0 Units
4 ▼ 200.0 mUnits/
▼ 146.5° mΩ -467.09 mΩ
V-BAND 50UM 3.5V 23MA

*
C
A
D
H



START 26.5000000008 GHz
STOP 40.0000000008 GHz

Figure 26. S-parameter plot of a 50 μ m FET. (a) at Ka-band (26.5 - 40 GHz).

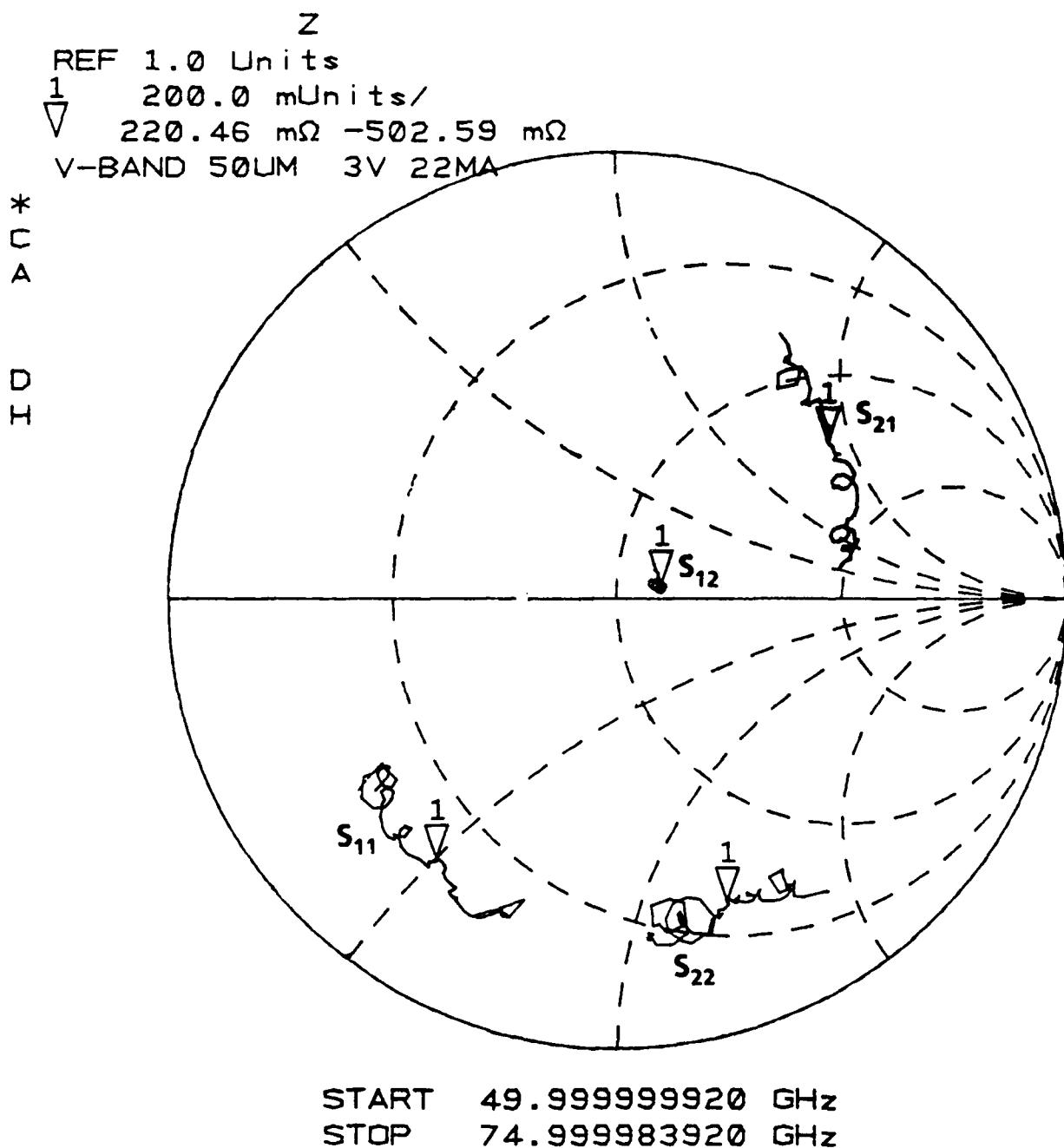


Figure 26. (b) at V-band (50 - 75 GHz).

MAXIMUM AVAILABLE GAIN OF V-BAND FET

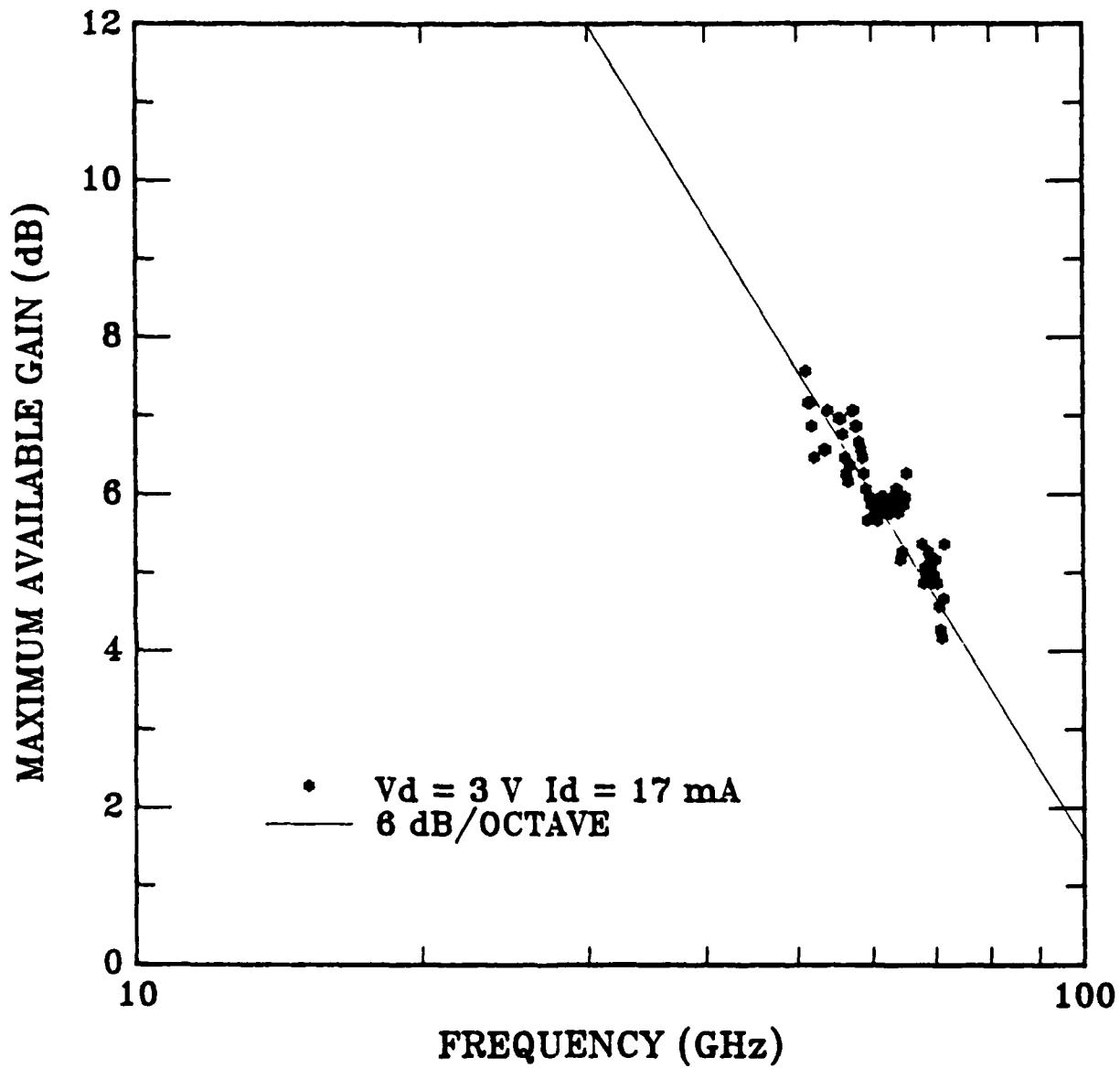


Figure 27. Maximum available gain vs frequency of a V-band FET.

SECTION VII
SUMMARY

Program achievements for the first 12-month period are summarized as follows:

- Optimized the quantum well MISFET layer structure using the numerical computer model.
- Developed the device processes, now nearly complete.
- Optimized pseudomorphic material growth conditions.
- Demonstrated MISFET operation at 60 GHz.
- Performed S-parameter measurements up to V-band.